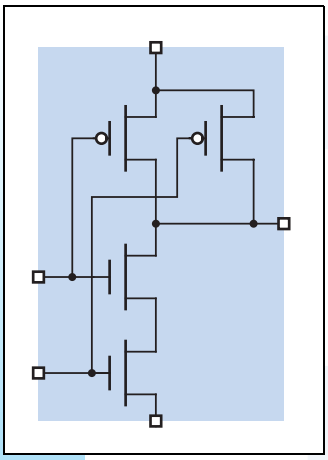


chapter 3

Digital Circuits

Marketing hype notwithstanding, we live in an analog world, not a digital one. Voltages, currents, and other physical quantities in real circuits take on values that are infinitely variable, depending on properties of the real devices that comprise the circuits. Because real values are continuously variable, we could use a physical quantity such as a signal voltage in a circuit to represent a real number (e.g., 3.14159265358979 volts represents the mathematical constant *pi* to 14 decimal digits of precision).

Unfortunately, stability and accuracy in physical quantities are difficult to obtain in real circuits. They are affected by manufacturing tolerances, temperature, power-supply voltage, cosmic rays, and noise created by other circuits, among other things. If we used an analog voltage to represent *pi*, we might find that instead of being an absolute mathematical constant, *pi* varied over a range of 10% or more.

Also, many mathematical and logical operations are difficult or impossible to perform with analog quantities. While it is possible with some cleverness to build an analog circuit whose output voltage is the square root of its input voltage, no one has ever built a 100-input, 100-output analog circuit whose outputs are a set of voltages identical to the set of input voltages, but sorted arithmetically.

The purpose of this chapter is to give you a solid working knowledge of the electrical aspects of digital circuits, enough for you to understand and

DO NOT COPY DO NOT COPY DO NOT COPY

Copyright © 1999 by John F. Wakerly Copying Prohibited

build real circuits and systems. We'll see in later chapters that with modern software tools, it's possible to "build" circuits in the abstract, using hardware design languages to specify their design and simulators to test their operation. Still, to build real, production-quality circuits, either at the board level or the chip level, you need to understand most of the material in this chapter. However, if you're anxious to start designing and simulating abstract circuits, you can just read the first section of this chapter and come back to the rest of it later.

3.1 Logic Signals and Gates

digital logic

Digital logic hides the pitfalls of the analog world by mapping the infinite set of real values for a physical quantity into two subsets corresponding to just two possible numbers or *logic values*—0 and 1. As a result, digital logic circuits can be analyzed and designed functionally, using switching algebra, tables, and other abstract means to describe the operation of well-behaved 0s and 1s in a circuit.

logic values

binary digit
bit

A logic value, 0 or 1, is often called a *binary digit*, or *bit*. If an application requires more than two discrete values, additional bits may be used, with a set of n bits representing 2^n different values.

Examples of the physical phenomena used to represent bits in some modern (and not-so-modern) digital technologies are given in Table 3-1. With most phenomena, there is an undefined region between the 0 and 1 states (e.g., voltage = 1.8 V, dim light, capacitor slightly charged, etc.). This undefined region is needed so that the 0 and 1 states can be unambiguously defined and reliably detected. Noise can more easily corrupt results if the boundaries separating the 0 and 1 states are too close.

LOW
HIGH

When discussing electronic logic circuits such as CMOS and TTL, digital designers often use the words "LOW" and "HIGH" in place of "0" and "1" to remind them that they are dealing with real circuits, not abstract quantities:

LOW A signal in the range of algebraically lower voltages, which is interpreted as a logic 0.

HIGH A signal in the range of algebraically higher voltages, which is interpreted as a logic 1.

Note that the assignments of 0 and 1 to LOW and HIGH are somewhat arbitrary. Assigning 0 to LOW and 1 to HIGH seems most natural, and is called *positive logic*. The opposite assignment, 1 to LOW and 0 to HIGH, is not often used, and is called *negative logic*.

positive logic
negative logic

Because a wide range of physical values represent the same binary value, digital logic is highly immune to component and power supply variations and noise. Furthermore, *buffer amplifier* circuits can be used to regenerate "weak" values into "strong" ones, so that digital signals can be transmitted over arbitrary distances without loss of information. For example, a buffer amplifier for CMOS

buffer amplifier

Copyright © 1999 by John F. Wakerly Copying Prohibited

Table 3-1 Physical states representing bits in different computer logic and memory technologies.

Technology	State Representing Bit	
	0	*1*
Pneumatic logic	Fluid at low pressure	Fluid at high pressure
Relay logic	Circuit open	Circuit closed
Complementary metal-oxide semi conductor (CMOS) logic	0–1.5 V	3.5–5.0 V
Transistor-transistor logic (TTL)	0–0.8 V	2.0–5.0 V
Fiber optics	Light off	Light on
Dynamic memory	Capacitor discharged	Capacitor charged
Nonvolatile, erasable memory	Electrons trapped	Electrons released
Bipolar read-only memory	Fuse blown	Fuse intact
Bubble memory	No magnetic bubble	Bubble present
Magnetic tape or disk	Flux direction “north”	Flux direction “south”
Polymer memory	Molecule in state A	Molecule in state B
Read-only compact disc	No pit	Pit
Rewriteable compact disc	Dye in crystalline state	Dye in non-crystalline state

logic converts any HIGH input voltage into an output very close to 5.0 V, and any LOW input voltage into an output very close to 0.0 V.

A logic circuit can be represented with a minimum amount of detail simply as a “black box” with a certain number of inputs and outputs. For example, Figure 3-1 shows a logic circuit with three inputs and one output. However, this representation does not describe how the circuit responds to input signals.

From the point of view of electronic circuit design, it takes a lot of information to describe the precise electrical behavior of a circuit. However, since the inputs of a digital logic circuit can be viewed as taking on only discrete 0 and 1 values, the circuit’s “logical” operation can be described with a table that ignores electrical behavior and lists only discrete 0 and 1 values.

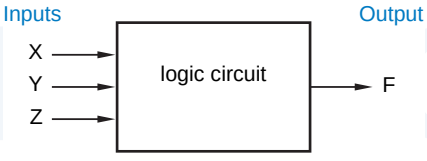


Figure 3-1
“Black box” representation of a three-input, one-output logic circuit.

Copyright © 1999 by John F. Wakerly Copying Prohibited

combinational circuit
truth table

A logic circuit whose outputs depend only on its current inputs is called a *combinational circuit*. Its operation is fully described by a *truth table* that lists all combinations of input values and the output value(s) produced by each one. Table 3-2 is the truth table for a logic circuit with three inputs X, Y, and Z and a single output F.

Table 3-2
Truth table for a combinational logic circuit.

X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

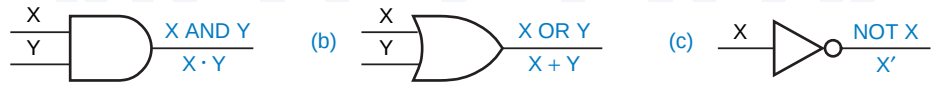
sequential circuit
state table

A circuit with memory, whose outputs depend on the current input *and* the sequence of past inputs, is called a *sequential circuit*. The behavior of such a circuit may be described by a *state table* that specifies its output and next state as functions of its current state and input. Sequential circuits will be introduced in \chapref{SeqPrinc}.

As we'll show in Section 4.1, just three basic logic functions, AND, OR, and NOT, can be used to build any combinational digital logic circuit. Figure 3-2 shows the truth tables and symbols for logic "gates" that perform these functions. The symbols and truth tables for AND and OR may be extended to gates with any number of inputs. The gates' functions are easily defined in words:

AND gate
OR gate
NOT gate
inverter

- An *AND gate* produces a 1 output if and only if all of its inputs are 1.
- An *OR gate* produces a 1 if and only if one or more of its inputs are 1.
- A *NOT gate*, usually called an *inverter*, produces an output value that is the opposite of its input value.



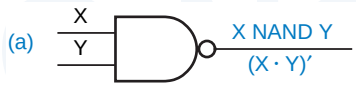
X	Y	X AND Y
0	0	0
0	1	0
1	0	0
1	1	1

X	Y	X OR Y
0	0	0
0	1	1
1	0	1
1	1	1

X	NOT X
0	1
1	0

Figure 3-2
Basic logic elements: (a) AND; (b) OR; (c) NOT(inverter).

Copyright © 1999 by John F. Wakerly Copying Prohibited



X	Y	X NAND Y
0	0	1
0	1	1
1	0	1
1	1	0

X	Y	X NOR Y
0	0	1
0	1	0
1	0	0
1	1	0

Figure 3-3
Inverting gates: (a) NAND; (b) NOR.

The circle on the inverter symbol's output is called an *inversion bubble*, and is used in this and other gate symbols to denote "inverting" behavior.

inversion bubble

Notice that in the definitions of AND and OR functions, we only had to state the input conditions for which the output is 1, because there is only one possibility when the output is not 1—it must be 0.

Two more logic functions are obtained by combining NOT with an AND or OR function in a single gate. Figure 3-3 shows the truth tables and symbols for these gates; Their functions are also easily described in words:

- A *NAND gate* produces the opposite of an AND gate's output, a 0 if and only if all of its inputs are 1.
- A *NOR gate* produces the opposite of an OR gate's output, a 0 if and only if one or more of its inputs are 1.

NAND gate

NOR gate

As with AND and OR gates, the symbols and truth tables for NAND and NOR may be extended to gates with any number of inputs.

Figure 3-4 is a logic circuit using AND, OR, and NOT gates that functions according to the truth table of Table 3-2. In Chapter 4 you'll learn how to go from a truth table to a logic circuit, and vice versa, and you'll also learn about the switching-algebra notation used in Figures 3-2 through 3-4.

Real logic circuits also function in another analog dimension—time. For example, Figure 3-5 is a *timing diagram* that shows how the circuit of Figure 3-4 might respond to a time-varying pattern of input signals. The timing diagram shows that the logic signals do not change between 0 and 1 instantaneously, and also that there is a lag between an input change and the corresponding output

timing diagram

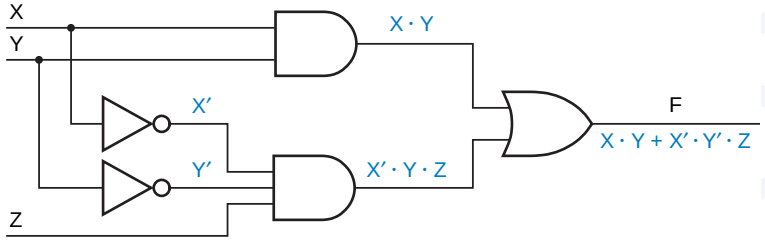


Figure 3-4
Logic circuit with the truth table of Table 3-2.

Copyright © 1999 by John F. Wakerly Copying Prohibited

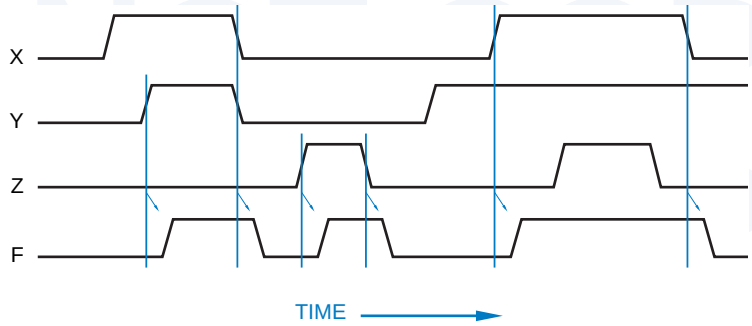


Figure 3-5
Timing diagram for a logic circuit.

change. Later in this chapter, you'll learn some of the reasons for this timing behavior, and how it is specified and handled in real circuits. And once again, you'll learn in a later chapter how this analog timing behavior can be generally ignored in most sequential circuits, and instead the circuit can be viewed as moving between discrete states at precise intervals defined by a clock signal.

Thus, even if you know nothing about analog electronics, you should be able to understand the logical behavior of digital circuits. However, there comes a time in design and debugging when every digital logic designer must temporarily throw out "the digital abstraction" and consider the analog phenomena that limit or disrupt digital performance. The rest of this chapter prepares you for that day by discussing the electrical characteristics of digital logic circuits.

THERE'S HOPE FOR NON-EE'S

If all of this electrical "stuff" bothers you, don't worry, at least for now. The rest of this book is written to be as independent of this stuff as possible. But you'll need it later, if you ever have to design and build digital systems in the real world.

3.2 Logic Families

There are many, many ways to design an electronic logic circuit. The first electrically controlled logic circuits, developed at Bell Laboratories in 1930s, were based on relays. In the mid-1940s, the first electronic digital computer, the Eniac, used logic circuits based on vacuum tubes. The Eniac had about 18,000 tubes and a similar number of logic gates, not a lot by today's standards of microprocessor chips with tens of millions of transistors. However, the Eniac could hurt you a lot more than a chip could if it fell on you—it was 100 feet long, 10 feet high, 3 feet deep, and consumed 140,000 watts of power!

semiconductor diode
bipolar junction transistor

The inventions of the *semiconductor diode* and the *bipolar junction transistor* allowed the development of smaller, faster, and more capable computers in the late 1950s. In the 1960s, the invention of the *integrated circuit (IC)*

Copyright © 1999 by John F. Wakerly Copying Prohibited

allowed multiple diodes, transistors, and other components to be fabricated on a single chip, and computers got still better.

integrated circuit (IC)

The 1960s also saw the introduction of the first integrated-circuit logic families. A *logic family* is a collection of different integrated-circuit chips that have similar input, output, and internal circuit characteristics, but that perform different logic functions. Chips from the same family can be interconnected to perform any desired logic function. On the other hand, chips from differing families may not be compatible; they may use different power-supply voltages or may use different input and output conditions to represent logic values.

logic family

The most successful *bipolar logic family* (one based on bipolar junction transistors) is *transistor-transistor logic (TTL)*. First introduced in the 1960s, TTL now is actually a family of logic families that are compatible with each other but differ in speed, power consumption, and cost. Digital systems can mix components from several different TTL families, according to design goals and constraints in different parts of the system. Although TTL was largely replaced by CMOS in the 1990s, you're still likely to encounter TTL components in academic labs; therefore, we introduce TTL families in Section 3.10.

bipolar logic family

transistor-transistor logic (TTL)

Ten years *before* the bipolar junction transistor was invented, the principles of operation were patented for another type of transistor, called the *metal-oxide semiconductor field effect transistor (MOSFET)*, or simply *MOS transistor*. However, MOS transistors were difficult to fabricate in the early days, and it wasn't until the 1960s that a wave of developments made MOS-based logic and memory circuits practical. Even then, MOS circuits lagged bipolar circuits considerably in speed, and were attractive only in selected applications because of their lower power consumption and higher levels of integration.

metal-oxide semiconductor field effect transistor (MOSFET)

MOS transistor

Beginning in the mid-1980s, advances in the design of MOS circuits, in particular *complementary MOS (CMOS)* circuits, vastly increased their performance and popularity. By far the majority of new large-scale integrated circuits, such as microprocessors and memories, use CMOS. Likewise, small- to medium-scale applications, for which TTL was once the logic family of choice, are now likely to use CMOS devices with equivalent functionality but higher speed and lower power consumption. CMOS circuits now account for the vast majority of the worldwide IC market.

complementary MOS (CMOS)

CMOS logic is both the most capable and the easiest to understand commercial digital logic technology. Beginning in the next section, we describe the basic structure of CMOS logic circuits and introduce the most commonly used commercial CMOS logic families.

GREEN STUFF Nowadays, the acronym "MOS" is usually spoken as "moss," rather than spelled out. And "CMOS" has always been spoken as "sea moss."

Copyright © 1999 by John F. Wakerly Copying Prohibited

As a consequence of the industry's transition from TTL to CMOS over a long period of time, many CMOS families were designed to be somewhat compatible with TTL. In Section 3.12, we show how TTL and CMOS families can be mixed within a single system.

3.3 CMOS Logic

The functional behavior of a CMOS logic circuit is fairly easy to understand, even if your knowledge of analog electronics is not particularly deep. The basic (and typically only) building blocks in CMOS logic circuits are MOS transistors, described shortly. Before introducing MOS transistors and CMOS logic circuits, we must talk about logic levels.

3.3.1 CMOS Logic Levels

Abstract logic elements process binary digits, 0 and 1. However, real logic circuits process electrical signals such as voltage levels. In any logic circuit, there is a range of voltages (or other circuit conditions) that is interpreted as a logic 0, and another, nonoverlapping range that is interpreted as a logic 1.

A typical CMOS logic circuit operates from a 5-volt power supply. Such a circuit may interpret any voltage in the range 0–1.5 V as a logic 0, and in the range 3.5–5.0 V as a logic 1. Thus, the definitions of LOW and HIGH for 5-volt CMOS logic are as shown in Figure 3-6. Voltages in the intermediate range (1.5–3.5 V) are not expected to occur except during signal transitions, and yield undefined logic values (i.e., a circuit may interpret them as either 0 or 1). CMOS circuits using other power supply voltages, such as 3.3 or 2.7 volts, partition the voltage range similarly.

3.3.2 MOS Transistors

A MOS transistor can be modeled as a 3-terminal device that acts like a voltage-controlled resistance. As suggested by Figure 3-7, an input voltage applied to one terminal controls the resistance between the remaining two terminals. In digital logic applications, a MOS transistor is operated so its resistance is always either very high (and the transistor is "off") or very low (and the transistor is "on").

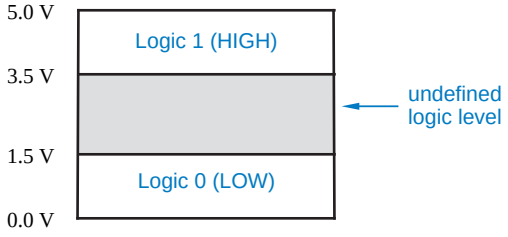


Figure 3-6
Logic levels for typical CMOS logic circuits.

Copyright © 1999 by John F. Wakerly Copying Prohibited

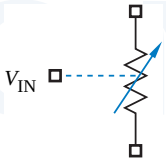
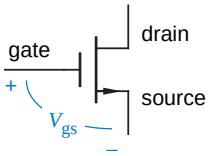


Figure 3-7
The MOS transistor as a voltage-controlled resistance.

There are two types of MOS transistors, *n*-channel and *p*-channel; the names refer to the type of semiconductor material used for the resistance-controlled terminals. The circuit symbol for an *n-channel MOS (NMOS) transistor* is shown in Figure 3-8. The terminals are called *gate*, *source*, and *drain*. (Note that the "gate" of a MOS transistor has nothing to do with a "logic gate.") As you might guess from the orientation of the circuit symbol, the drain is normally at a higher voltage than the source.

n-channel MOS (NMOS) transistor
gate
source
drain



Voltage-controlled resistance:
increase V_{gs} ==> decrease R_{ds}

Note: normally, $V_{gs} \geq 0$

Figure 3-8
Circuit symbol for an n-channel MOS (NMOS) transistor.

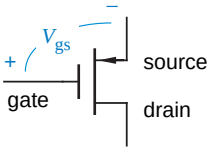
The voltage from gate to source (V_{gs}) in an NMOS transistor is normally zero or positive. If $V_{gs} = 0$, then the resistance from drain to source (R_{ds}) is very high, on the order of a megohm (10^6 ohms) or more. As we increase V_{gs} (i.e., increase the voltage on the gate), R_{ds} decreases to a very low value, 10 ohms or less in some devices.

The circuit symbol for a *p-channel MOS (PMOS) transistor* is shown in Figure 3-9. Operation is analogous to that of an NMOS transistor, except that the source is normally at a higher voltage than the drain, and V_{gs} is normally zero or negative. If V_{gs} is zero, then the resistance from source to drain (R_{ds}) is very high. As we algebraically decrease V_{gs} (i.e., *decrease* the voltage on the gate), R_{ds} decreases to a very low value.

p-channel MOS (PMOS) transistor

The gate of a MOS transistor has a very high impedance. That is, the gate is separated from the source and the drain by an insulating material with a very high resistance. However, the gate voltage creates an electric field that enhances or retards the flow of current between source and drain. This is the "field effect" in the "MOSFET" name.

Regardless of gate voltage, almost no current flows from the gate to source, or from the gate to drain for that matter. The resistance between the gate and the



Voltage-controlled resistance:
decrease V_{gs} ==> decrease R_{ds}

Note: normally, $V_{gs} \leq 0$

Figure 3-9
Circuit symbol for a *p*-channel MOS (PMOS) transistor.

Copyright © 1999 by John F. Wakerly Copying Prohibited

IMPEDANCE VS. RESISTANCE Technically, there's a difference between "impedance" and "resistance," but electrical engineers often use the terms interchangeably. So do we in this text.

other terminals of the device is extremely high, well over a megohm. The small amount of current that flows across this resistance is very small, typically less than one microampere (μA, 10^{-6} A), and is called a *leakage current.*

leakage current

The MOS transistor symbol itself reminds us that there is no connection between the gate and the other two terminals of the device. However, the gate of a MOS transistor is capacitively coupled to the source and drain, as the symbol might suggest. In high-speed circuits, the power needed to charge and discharge this capacitance on each input-signal transition accounts for a nontrivial portion of a circuit's power consumption.

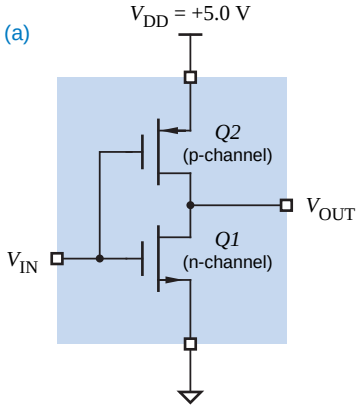
3.3.3 Basic CMOS Inverter Circuit

CMOS logic

NMOS and PMOS transistors are used together in a complementary way to form *CMOS logic*. The simplest CMOS circuit, a logic inverter, requires only one of each type of transistor, connected as shown in Figure 3-10(a). The power supply voltage, V_{DD}, typically may be in the range 2–6 V, and is most often set at 5.0 V for compatibility with TTL circuits.

Ideally, the functional behavior of the CMOS inverter circuit can be characterized by just two cases tabulated in Figure 3-10(b):

1. V_{IN} is 0.0 V. In this case, the bottom, *n*-channel transistor *Q1* is off, since its V_{gs} is 0, but the top, *p*-channel transistor *Q2* is on, since its V_{gs} is a large negative value (–5.0 V). Therefore, *Q2* presents only a small resistance between the power supply terminal (V_{DD}, +5.0 V) and the output terminal (V_{OUT}), and the output voltage is 5.0 V.



(b)

V_{IN}	Q1	Q2	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

(c)

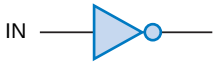


Figure 3-10
CMOS inverter:
(a) circuit diagram;
(b) functional behavior;
(c) logic symbol.

Copyright © 1999 by John F. Wakerly Copying Prohibited

2. V_{IN} is 5.0 V. Here, *Q1* is on, since its V_{gs} is a large positive value (+5.0 V), but *Q2* is off, since its V_{gs} is 0. Thus, *Q1* presents a small resistance between the output terminal and ground, and the output voltage is 0 V.

With the foregoing functional behavior, the circuit clearly behaves as a logical inverter, since a 0-volt input produces a 5-volt output, and vice versa

Another way to visualize CMOS operation uses switches. As shown in Figure 3-11(a), the *n*-channel (bottom) transistor is modeled by a normally-open switch, and the *p*-channel (top) transistor by a normally-closed switch. Applying a HIGH voltage changes each switch to the opposite of its normal state, as shown in (b).

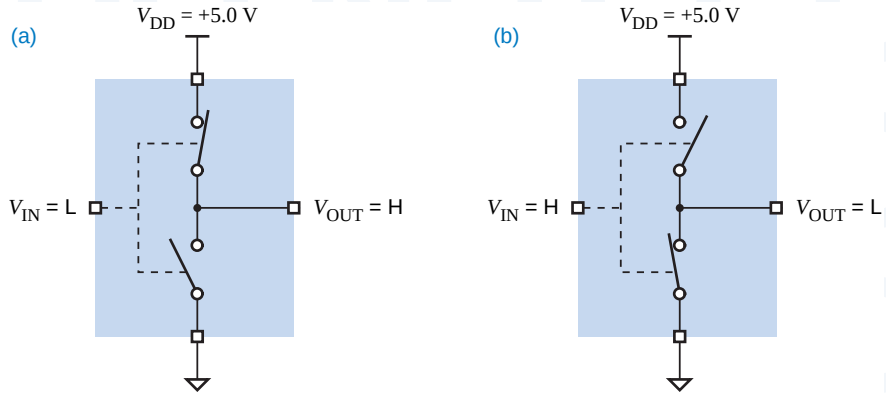


Figure 3-11
Switch model for CMOS inverter: (a) LOW input; (b) HIGH input.

The switch model gives rise to a way of drawing CMOS circuits that makes their logical behavior more readily apparent. As shown in Figure 3-12, different symbols are used for the *p*- and *n*-channel transistors to reflect their logical behavior. The *n*-channel transistor (*Q1*) is switched "on," and current flows between source and drain, when a HIGH voltage is applied to its gate; this seems natural enough. The *p*-channel transistor (*Q2*) has the opposite behavior. It is

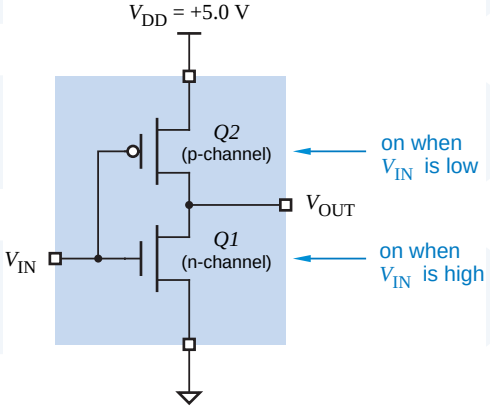


Figure 3-12
CMOS inverter logical operation.

Copyright © 1999 by John F. Wakerly Copying Prohibited

WHAT'S IN A NAME?

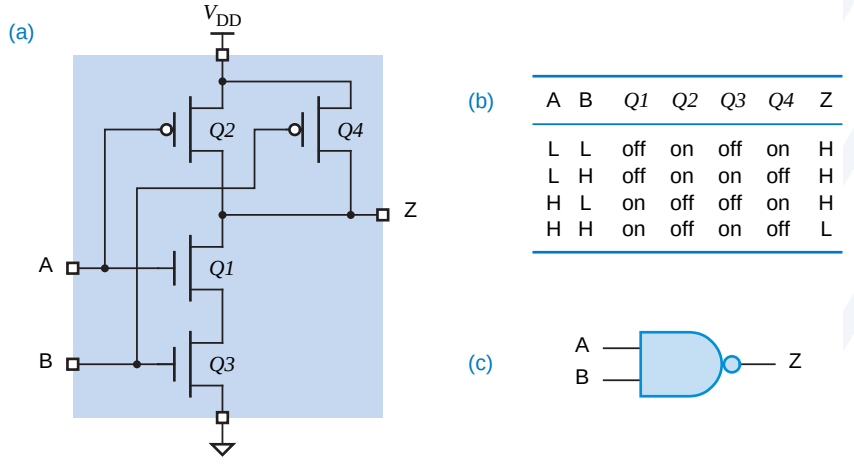
The "DD" in the name "V_{DD}" refers to the *drain* terminal of an MOS transistor. This may seem strange, since in the CMOS inverter V_{DD} is actually connected to the *source* terminal of a PMOS transistor. However, CMOS logic circuits evolved from NMOS logic circuits, where the supply *was* connected to the drain of an NMOS transistor through a load resistor, and the name "V_{DD}" stuck. Also note that ground is sometimes referred to as "V_{SS}" in CMOS and NMOS circuits. Some authors and most circuit manufacturers use "V_{CC}" as the symbol for the CMOS supply voltage, since this name is used in TTL circuits, which historically preceded CMOS. To get you used to both, we'll start using "V_{CC}" in Section 3.4.

"on" when a LOW voltage is applied; the inversion bubble on its gate indicates this inverting behavior.

3.3.4 CMOS NAND and NOR Gates

Both NAND and NOR gates can be constructed using CMOS. A *k*-input gate uses *k* *p*-channel and *k* *n*-channel transistors. Figure 3-13 shows a 2-input CMOS NAND gate. If either input is LOW, the output Z has a low-impedance connection to V_{DD} through the corresponding "on" *p*-channel transistor, and the path to ground is blocked by the corresponding "off" *n*-channel transistor. If both inputs are HIGH, the path to V_{DD} is blocked, and Z has a low-impedance connection to ground. Figure 3-14 shows the switch model for the NAND gate's operation.

Figure 3-15 shows a CMOS NOR gate. If both inputs are LOW, the output Z has a low-impedance connection to V_{DD} through the "on" *p*-channel transistors, and the path to ground is blocked by the "off" *n*-channel transistors. If either input is HIGH, the path to V_{DD} is blocked, and Z has a low-impedance connection to ground.



A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L

Figure 3-13 CMOS 2-input NAND gate: (a) circuit diagram; (b) function table; (c) logic symbol.

Copyright © 1999 by John F. Wakerly Copying Prohibited

NAND VS. NOR CMOS NAND and NOR gates do not have identical performance. For a given silicon area, an *n*-channel transistor has lower "on" resistance than a *p*-channel transistor. Therefore, when transistors are put in series, *k* *n*-channel transistors have lower "on" resistance than do *k* *p*-channel ones. As a result, a *k*-input NAND gate is generally faster than and preferred over a *k*-input NOR gate.

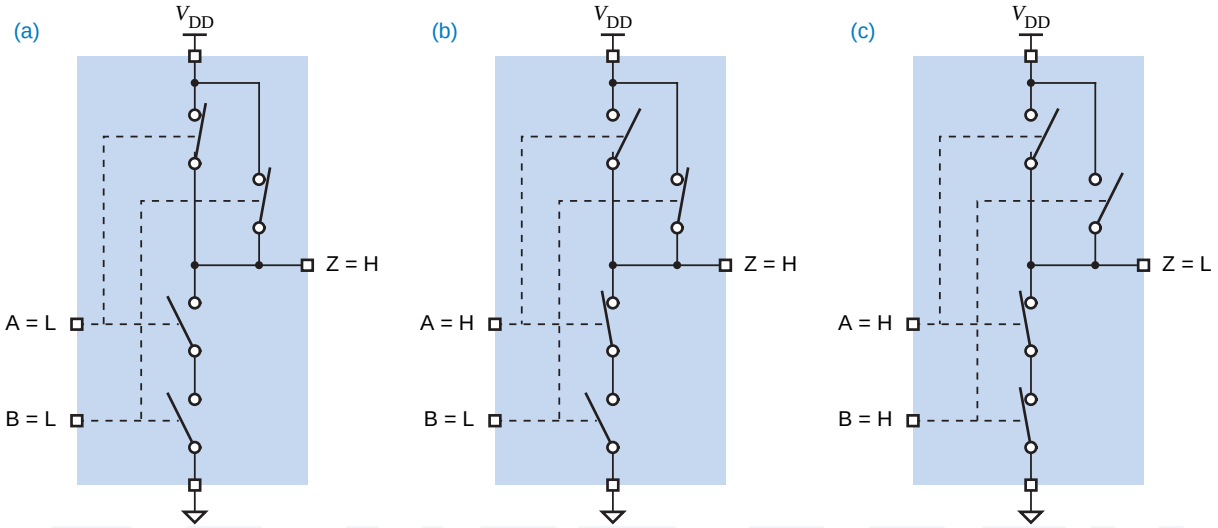
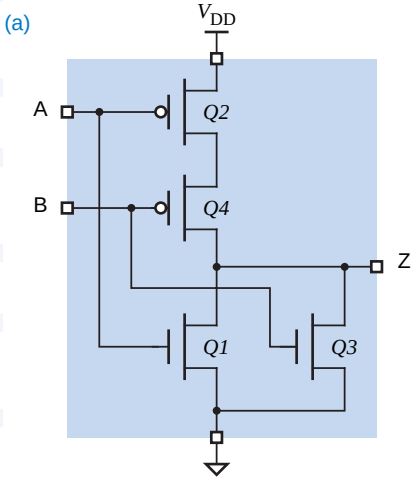


Figure 3-14 Switch model for CMOS 2-input NAND gate: (a) both inputs LOW; (b) one input HIGH; (c) both inputs HIGH.



(b)

A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

(c)

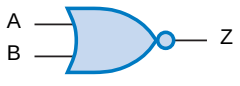
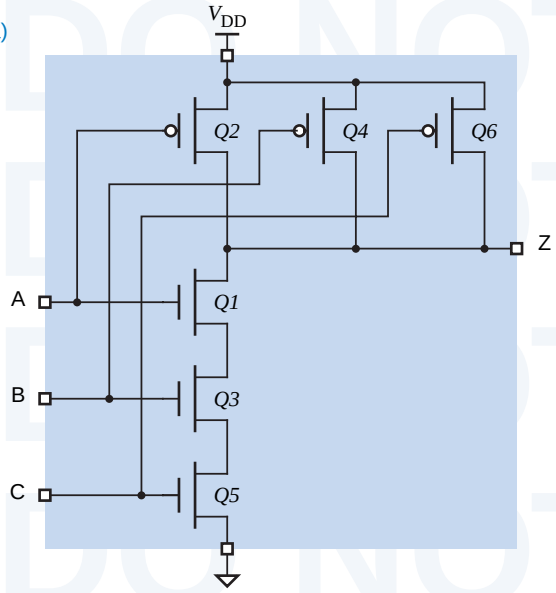


Figure 3-15 CMOS 2-input NOR gate: (a) circuit diagram; (b) function table; (c) logic symbol.

Copyright © 1999 by John F. Wakerly Copying Prohibited

(a)



(b)

A	B	C	Q1	Q2	Q3	Q4	Q5	Q6	Z
L	L	L	off	on	off	on	off	on	H
L	L	H	off	on	off	on	on	off	H
L	H	L	off	on	on	off	off	on	H
L	H	H	off	on	on	off	on	off	H
H	L	L	on	off	off	on	off	on	H
H	L	H	on	off	off	on	on	off	H
H	H	L	on	off	on	off	off	on	H
H	H	H	on	off	on	off	on	off	L

(c)

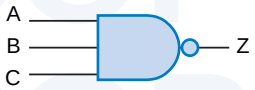


Figure 3-16 CMOS 3-input NAND gate: (a) circuit diagram; (b) function table; (c) logic symbol.

3.3.5 Fan-In

fan-in

The number of inputs that a gate can have in a particular logic family is called the logic family's *fan-in*. CMOS gates with more than two inputs can be obtained by extending series-parallel designs on Figures 3-13 and 3-15 in the obvious manner. For example, Figure 3-16 shows a 3-input CMOS NAND gate.

In principle, you could design a CMOS NAND or NOR gate with a very large number of inputs. In practice, however, the additive "on" resistance of series transistors limits the fan-in of CMOS gates, typically to 4 for NOR gates and 6 for NAND gates.

As the number of inputs is increased, CMOS gate designers may compensate by increasing the size of the series transistors to reduce their resistance and the corresponding switching delay. However, at some point this becomes inefficient or impractical. Gates with a large number of inputs can be made faster and smaller by cascading gates with fewer inputs. For example, Figure 3-17 shows

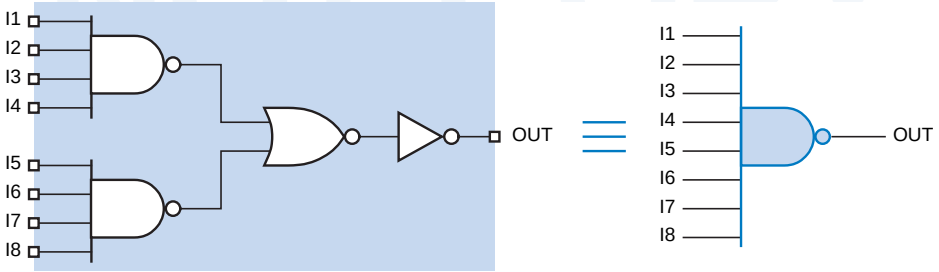
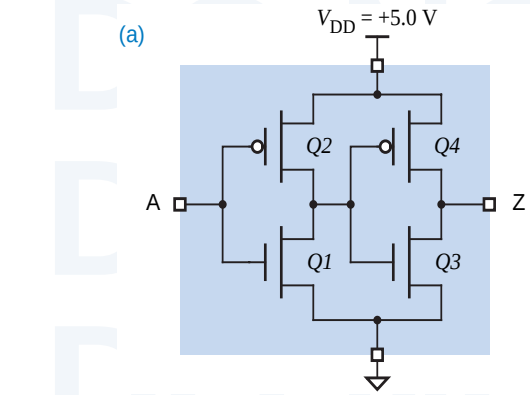


Figure 3-17 Logic diagram equivalent to the internal structure of an 8-input CMOS NAND gate.

Copyright © 1999 by John F. Wakerly Copying Prohibited



(b)

A	Q1	Q2	Q3	Q4	Z
L	off	on	on	off	L
H	on	off	off	on	H

(c)

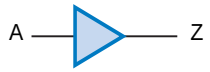


Figure 3-18 CMOS noninverting buffer: (a) circuit diagram; (b) function table; (c) logic symbol.

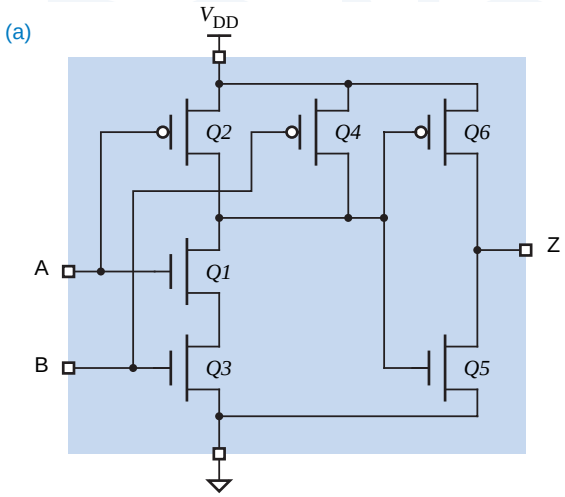
the logical structure of an 8-input CMOS NAND gate. The total delay through a 4-input NAND, a 2-input NOR, and an inverter is typically less than the delay of a one-level 8-input NAND circuit.

3.3.6 Noninverting Gates

In CMOS, and in most other logic families, the simplest gates are inverters, and the next simplest are NAND gates and NOR gates. A logical inversion comes "for free," and it typically is not possible to design a noninverting gate with a smaller number of transistors than an inverting one.

CMOS noninverting buffers and AND and OR gates are obtained by connecting an inverter to the output of the corresponding inverting gate. Combining Figure 3-15(a) with an inverter yields an OR gate. Thus, Figure 3-18 shows a noninverting buffer and Figure 3-19 shows an AND gate.

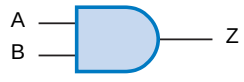
Figure 3-19 CMOS 2-input AND gate: (a) circuit diagram; (b) function table; (c) logic symbol.



(b)

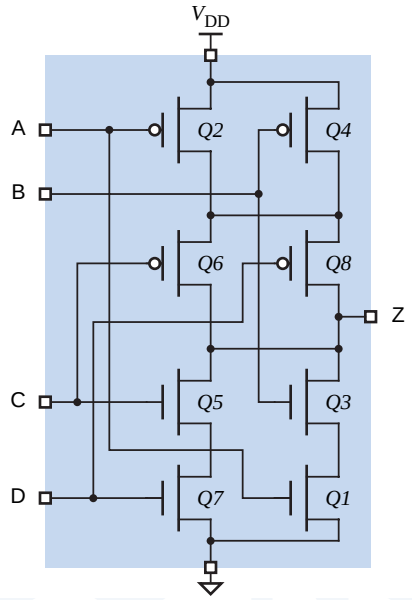
A	B	Q1	Q2	Q3	Q4	Q5	Q6	Z
L	L	off	on	off	on	on	off	L
L	H	off	on	on	off	on	off	L
H	L	on	off	off	on	on	off	L
H	H	on	off	on	off	off	on	H

(c)



Copyright © 1999 by John F. Wakerly Copying Prohibited

(a)



(b)

A	B	C	D	*Q1*	*Q2*	*Q3*	*Q4*	*Q5*	*Q6*	*Q7*	*Q8*	Z
L	L	L	L	off	on	off	on	off	on	off	on	H
L	L	L	H	off	on	off	on	off	on	on	off	H
L	L	H	L	off	on	off	on	on	off	off	on	H
L	L	H	H	off	on	off	on	on	off	on	off	L
L	H	L	L	off	on	on	off	off	on	off	on	H
L	H	L	H	off	on	on	off	off	on	on	off	H
L	H	H	L	off	on	on	off	on	off	off	on	H
L	H	H	H	off	on	on	off	on	off	on	off	L
H	L	L	L	on	off	off	on	off	on	off	on	H
H	L	L	H	on	off	off	on	off	on	on	off	H
H	L	H	L	on	off	off	on	on	off	off	on	H
H	L	H	H	on	off	off	on	on	off	on	off	L
H	H	L	L	on	off	on	off	off	on	off	on	L
H	H	L	H	on	off	on	off	off	on	on	off	L
H	H	H	L	on	off	on	off	on	off	off	on	L
H	H	H	H	on	off	on	off	on	off	on	off	L

Figure 3-20 CMOS AND-OR-INVERT gate: (a) circuit diagram; (b) function tab

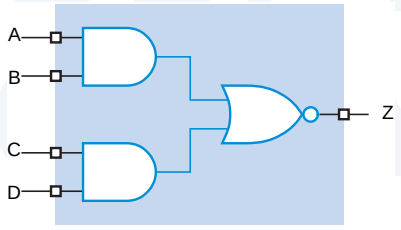
3.3.7 CMOS AND-OR-INVERT and OR-AND-INVERT Gates

AND-OR-INVERT (AOI) gate

CMOS circuits can perform two levels of logic with just a single "level" of transistors. For example, the circuit in Figure 3-20(a) is a two-wide, two-input CMOS *AND-OR-INVERT (AOI) gate*. The function table for this circuit is shown in (b) and a logic diagram for this function using AND and NOR gates is shown in Figure 3-21. Transistors can be added to or removed from this circuit to obtain an AOI function with a different number of ANDs or a different number of inputs per AND.

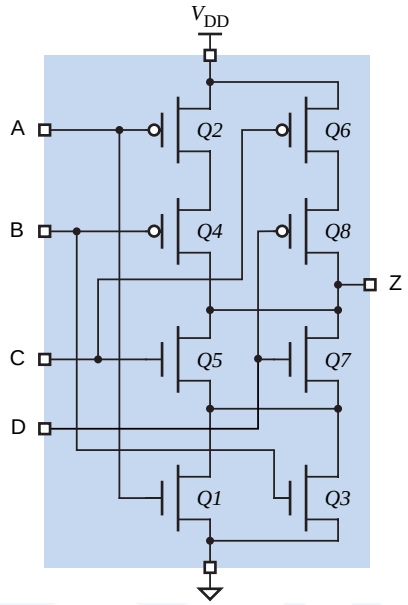
The contents of each of the *Q1–Q8* columns in Figure 3-20(b) depends only on the input signal connected to the corresponding transistor's gate. The last column is constructed by examining each input combination and determining whether Z is connected to V_{DD} or ground by "on" transistors for that input combination. Note that Z is never connected to *both* V_{DD} and ground for any input combination; in such a case the output would be a non-logic value some-

Figure 3-21
Logic diagram for CMOS AND-OR-INVERT gate.



Copyright © 1999 by John F. Wakerly Copying Prohibited

(a)



(b)

A	B	C	D	*Q1*	*Q2*	*Q3*	*Q4*	*Q5*	*Q6*	*Q7*	*Q8*	Z
L	L	L	L	off	on	off	on	off	on	off	on	H
L	L	L	H	off	on	off	on	off	on	on	off	H
L	L	H	L	off	on	off	on	on	off	off	on	H
L	L	H	H	off	on	off	on	on	off	on	off	H
L	H	L	L	off	on	on	off	off	on	off	on	H
L	H	L	H	off	on	on	off	off	on	on	off	L
L	H	H	L	off	on	on	off	on	off	off	on	L
L	H	H	H	off	on	on	off	on	off	on	off	L
H	L	L	L	on	off	off	on	off	on	off	on	H
H	L	L	H	on	off	off	on	off	on	on	off	L
H	L	H	L	on	off	off	on	on	off	off	on	L
H	L	H	H	on	off	off	on	on	off	on	off	L
H	H	L	L	on	off	on	off	off	on	off	on	H
H	H	L	H	on	off	on	off	off	on	on	off	L
H	H	H	L	on	off	on	off	on	off	off	on	L
H	H	H	H	on	off	on	off	on	off	on	off	L

Figure 3-22 CMOS OR-AND-INVERT gate: (a) circuit diagram; (b) function table.

where between LOW and HIGH, and the output structure would consume excessive power due to the low-impedance connection between V_{DD} and ground.

A circuit can also be designed to perform an OR-AND-INVERT function. For example, Figure 3-22(a) is a two-wide, two-input CMOS *OR-AND-INVERT (OAI) gate*. The function table for this circuit is shown in (b); the values in each column are determined just as we did for the CMOS AOI gate. A logic diagram for the OAI function using OR and NAND gates is shown in Figure 3-23.

OR-AND-INVERT (AOI) gate

The speed and other electrical characteristics of a CMOS AOI or OAI gate are quite comparable to those of a single CMOS NAND or NOR gate. As a result, these gates are very appealing because they can perform two levels of logic (AND-OR or OR-AND) with just one level of delay. Most digital designers don't bother to use AOI gates in their discrete designs. However, CMOS VLSI devices often use these gates internally, since many HDL synthesis tools can automatically convert AND/OR logic into AOI gates when appropriate.

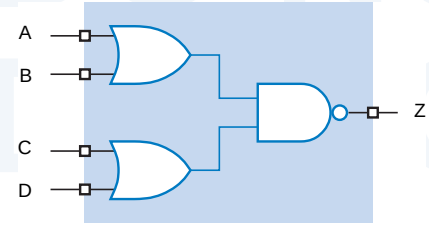


Figure 3-23
Logic diagram for CMOS OR-AND-INVERT gate.

Copyright © 1999 by John F. Wakerly Copying Prohibited

3.4 Electrical Behavior of CMOS Circuits

The next three sections discuss electrical, not logical, aspects of CMOS circuit operation. It's important to understand this material when you design real circuits using CMOS or other logic families. Most of this material is aimed at providing a framework for ensuring that the "digital abstraction" is really valid for a given circuit. In particular, a circuit or system designer must provide in a number of areas adequate engineering design margins—insurance that the circuit will work properly even under the worst of conditions.

engineering design margins

3.4.1 Overview

The topics that we discuss in Sections 3.5–3.7 include the following:

- *Logic voltage levels*. CMOS devices operating under normal conditions are guaranteed to produce output voltage levels within well-defined LOW and HIGH ranges. And they recognize LOW and HIGH input voltage levels over somewhat wider ranges. CMOS manufacturers specify these ranges and operating conditions very carefully to ensure compatibility among different devices in the same family, and to provide a degree of interoperability (if you're careful) among devices in different families.
- *DC noise margins*. Nonnegative DC noise margins ensure that the highest LOW voltage produced by an output is always lower than the highest voltage that an input can reliably interpret as LOW, and that the lowest HIGH voltage produced by an output is always higher than the lowest voltage that an input can reliably interpret as HIGH. A good understanding of noise margins is especially important in circuits that use devices from a number of different families.
- *Fanout*. This refers to the number and type of inputs that are connected to a given output. If too many inputs are connected to an output, the DC noise margins of the circuit may be inadequate. Fanout may also affect the speed at which the output changes from one state to another.
- *Speed*. The time that it takes a CMOS output to change from the LOW state to the HIGH state, or vice versa, depends on both the internal structure of the device and the characteristics of the other devices that it drives, even to the extent of being affected by the wire or printed-circuit-board traces connected to the output. We'll look at two separate components of "speed"—transition time and propagation delay.
- *Power consumption*. The power consumed by a CMOS device depends on a number of factors, including not only its internal structure, but also the input signals that it receives, the other devices that it drives, and how often its output changes between LOW and HIGH.

Copyright © 1999 by John F. Wakerly Copying Prohibited

- *Noise.* The main reason for providing engineering design margins is to ensure proper circuit operation in the presence of noise. Noise can be generated by a number of sources; several of them are listed below, from the least likely to the (perhaps surprisingly) most likely:
  - Cosmic rays.
  - Magnetic fields from nearby machinery.
  - Power-supply disturbances.
  - The switching action of the logic circuits themselves.
- *Electrostatic discharge.* Would you believe that you can destroy a CMOS device just by touching it?
- *Open-drain outputs.* Some CMOS outputs omit the usual *p*-channel pull-up transistors. In the HIGH state, such outputs are effectively a "no-connection," which is useful in some applications.
- *Three-state outputs.* Some CMOS devices have an extra "output enable" control input that can be used to disable both the *p*-channel pull-up transistors and the *n*-channel pull-down transistors. Many such device outputs can be tied together to create a multisource bus, as long as the control logic is arranged so that at most one output is enabled at a time.

3.4.2 Data Sheets and Specifications

data sheet

The manufacturers of real-world devices provide *data sheets* that specify the devices' logical and electrical characteristics. The electrical specifications portion of a minimal data sheet for a simple CMOS device, the 54/74HC00 quadruple NAND gate, is shown in Table 3-3. Different manufacturers typically specify additional parameters, and they may vary in how they specify even the "standard" parameters shown in the table. Thus, they usually also show the test circuits and waveforms that they use to define various parameters, for example as shown in Figure 3-24. Note that this figure contains information for some parameters in addition to those used with the 54/74HC00.

Most of the terms in the data sheet and the waveforms in the figure are probably meaningless to you at this point. However, after reading the next three sections you should know enough about the electrical characteristics of CMOS circuits that you'll be able to understand the salient points of this or any other data sheet. As a logic designer, you'll need this knowledge to create reliable and robust real-world circuits and systems.

DON'T BE AFRAID Computer science students and other non-EE readers should not have undue fear of the material in the next three sections. Only a basic understanding of electronics, at about the level of Ohm's law, is required.

Copyright © 1999 by John F. Wakerly Copying Prohibited

Table 3-3 Manufacturer's data sheet for a typical CMOS device, the 54/74HC00 quad NAND gate.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE
The following conditions apply unless otherwise specified:
Commercial: $T_A = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$

Sym.	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH level	Guaranteed logic HIGH level		3.15	—	—	V
V_{IL}	Input LOW level	Guaranteed logic LOW level		—	—	1.35	V
I_{IH}	Input HIGH current	V_{CC} = Max., $V_I = V_{CC}$		—	—	1	μA
I_{IL}	Input LOW current	V_{CC} = Max., V_I = 0 V		—	—	−1	μA
V_{IK}	Clamp diode voltage	V_{CC} = Min., I_N = −18 mA		—	−0.7	−1.2	V
I_{IOS}	Short-circuit current	V_{CC} = Max.,[3] V_O = GND		—	—	−35	mA
V_{OH}	Output HIGH voltage	V_{CC} = Min., $V_{IN} = V_{IL}$	I_{OH} = −20 µA	4.4	4.499	—	V
			I_{OH} = −4 mA	3.84	4.3	—	V
V_{OL}	Output LOW voltage	V_{CC} = Min. $V_{IN} = V_{IH}$	I_{OL} = 20 µA	—	.001	0.1	V
			I_{OL} = 4 mA		0.17	0.33	
I_{CC}	Quiescent power supply current	V_{CC} = Max. V_{IN} = GND or V_{CC}, I_O = 0		—	2	10	µA

SWITCHING CHARACTERISTICS OVER OPERATING RANGE, C_L = 50 pF

Sym.	Parameter[4]	Test Conditions		Min.	Typ.	Max.	Unit
t_{PD}	Propagation delay	A or B to Y		—	9	19	ns
C_I	Input capacitance	V_{IN} = 0 V		—	3	10	pF
C_{pd}	Power dissipation capacitance per gate		No load	—	22	—	pF

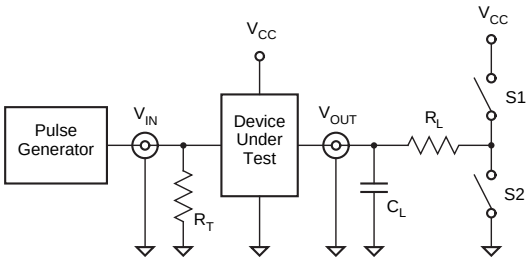
NOTES:

1. *For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.*
2. *Typical values are at V_{CC} = 5.0 V, +25°C ambient.*
3. *Not more than one output should be shorted at a time. Duration of short-circuit test should not exceed one second.*
4. *This parameter is guaranteed but not tested.*

WHAT'S IN A NUMBER? Two different prefixes, "74" and "54," are used in the part numbers of CMOS and TTL devices. These prefixes simply distinguish between commercial and military versions. A 74HC00 is the commercial part and the 54HC00 is the military version.

Copyright © 1999 by John F. Wakerly Copying Prohibited

TEST CIRCUIT FOR ALL OUTPUTS

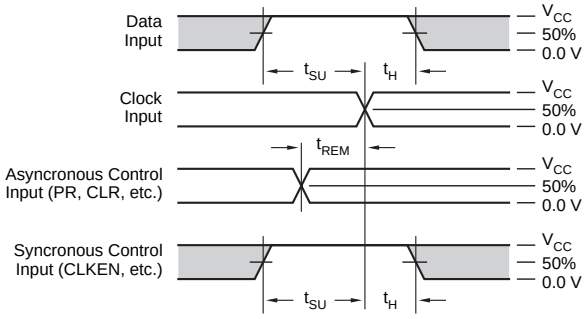


LOADING

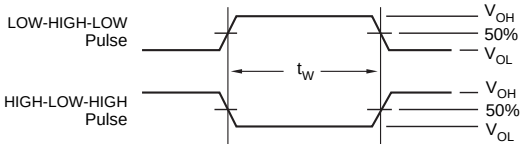
Parameter		R_L	C_L	S1	S2
t_{en}	t_{pZH}	1 KW	50 pF or 150 pF	Open	Closed
	t_{pZL}			Closed	Open
t_{dis}	t_{pHZ}	1 KW		Open	Closed
	t_{pLZ}			Closed	Open
t_{pd}		—	50 pF or 150 pF	Open	Open

DEFINITIONS:
C_L = Load capacitance, includes jig and probe capacitance.
R_T = Termination resistance, should equal Z_{OUT} of the Pulse Generator.

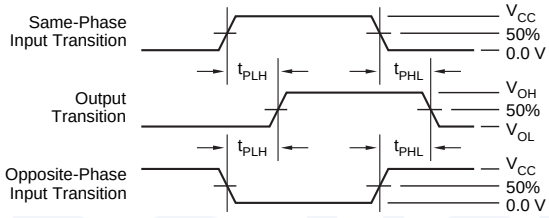
SETUP, HOLD, AND RELEASE TIMES



PULSE WIDTH



PROPAGATION DELAY



THREE-STATE ENABLE AND DISABLE TIMES

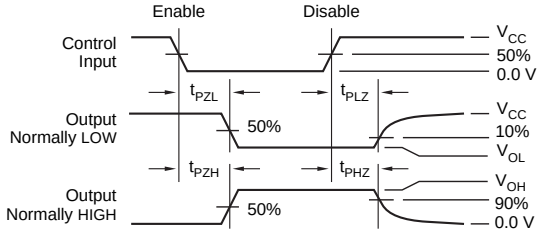


Figure 3-24 Test circuits and waveforms for HC-series logic.

3.5 CMOS Steady-State Electrical Behavior

This section discusses the steady-state behavior of CMOS circuits, that is, the circuits' behavior when inputs and outputs are not changing. The next section discusses dynamic behavior, including speed and power dissipation.

3.5.1 Logic Levels and Noise Margins

The table in Figure 3-10(b) on page 84 defined the CMOS inverter's behavior only at two discrete input voltages; other input voltages may yield different output voltages. The complete input-output transfer characteristic can be described

DO NOT COPY

Copyright © 1999 by John F. Wakerly Copying Prohibited

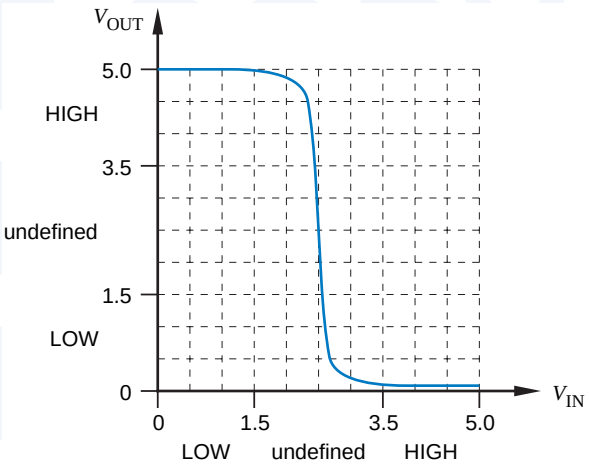


Figure 3-25
Typical input-output transfer characteristic of a CMOS inverter.

by a graph such as Figure 3-25. In this graph, the input voltage is varied from 0 to 5 V, as shown on the X axis; the Y axis plots the output voltage.

If we believed the curve in Figure 3-25, we could define a CMOS LOW input level as any voltage under 2.4 V, and a HIGH input level as anything over 2.6 V. Only when the input is between 2.4 and 2.6 V does the inverter produce a nonlogic output voltage under this definition.

Unfortunately, the typical transfer characteristic shown in Figure 3-25 is just that—typical, but not guaranteed. It varies greatly under different conditions of power supply voltage, temperature, and output loading. The transfer characteristic may even vary depending on when the device was fabricated. For example, after months of trying to figure out why gates made on some days were good and on other days were bad, one manufacturer discovered that the bad gates were victims of airborne contamination by a particularly noxious perfume worn by one of its production-line workers!

Sound engineering practice dictates that we use more conservative specifications for LOW and HIGH. The conservative specs for a typical CMOS logic family (HC-series) are depicted in Figure 3-26. These parameters are specified by CMOS device manufacturers in data sheets like Table 3-3, and are defined as follows:

V_{OHmin} The minimum output voltage in the HIGH state.

V_{IHmin} The minimum input voltage guaranteed to be recognized as a HIGH.

V_{ILmax} The maximum input voltage guaranteed to be recognized as a LOW.

V_{OLmax} The maximum output voltage in the LOW state.

The input voltages are determined mainly by switching thresholds of the two transistors, while the output voltages are determined mainly by the "on" resistance of the transistors.

Copyright © 1999 by John F. Wakerly Copying Prohibited

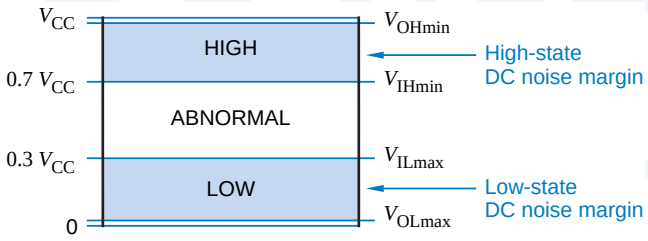


Figure 3-26
Logic levels and noise margins for the HC-series CMOS logic family.

All of the parameters in Figure 3-26 are guaranteed by CMOS manufacturers over a range of temperature and output loading. Parameters are also guaranteed over a range of power-supply voltage V_{CC}, typically 5.0 V±10%.

The data sheet in Table 3-3 on page 94 specifies values for each of these parameters for HC-series CMOS. Notice that there are two values specified for V_{OHmin} and V_{OLmax}, depending on whether the output current (I_{OH} or I_{OL}) is large or small. When the device outputs are connected only to other CMOS inputs, the output current is low (e.g, $I_{OL} \leq 20\ \mu A$), so there's very little voltage drop across the output transistors. In the next few subsections, we'll focus on these "pure" CMOS applications.

power-supply rails

The power-supply voltage V_{CC} and ground are often called the *power-supply rails*. CMOS levels are typically a function of the power-supply rails:

V_{OHmin} $V_{CC} - 0.1$ V
V_{IHmin} 70% of V_{CC}
V_{ILmax} 30% of V_{CC}
V_{OLmax} ground + 0.1 V

Notice in Table 3-3 that V_{OHmin} is specified as 4.4 V. This is only a 0.1-V drop from V_{CC}, since the worst-case number is specified with V_{CC} at its minimum value of 5.0–10% = 4.5 V.

DC noise margin

DC noise margin is a measure of how much noise it takes to corrupt a worst-case output voltage into a value that may not be recognized properly by an input. For HC-series CMOS in the LOW state, V_{ILmax} (1.35 V) exceeds V_{OLmax} (0.1 V) by 1.25 V so the LOW-state DC noise margin is 1.25 V. Likewise, there is DC noise margin of 1.25 V in the HIGH state. In general, CMOS outputs have excellent DC noise margins when driving other CMOS inputs.

Regardless of the voltage applied to the input of a CMOS inverter, the input consumes very little current, only the leakage current of the two transistors' gates. The maximum amount of current that can flow is also specified by the device manufacturer:

I_{IH} The maximum current that flows into the input in the LOW state.

I_{IL} The maximum current that flows into the input in the HIGH state.

Copyright © 1999 by John F. Wakerly Copying Prohibited

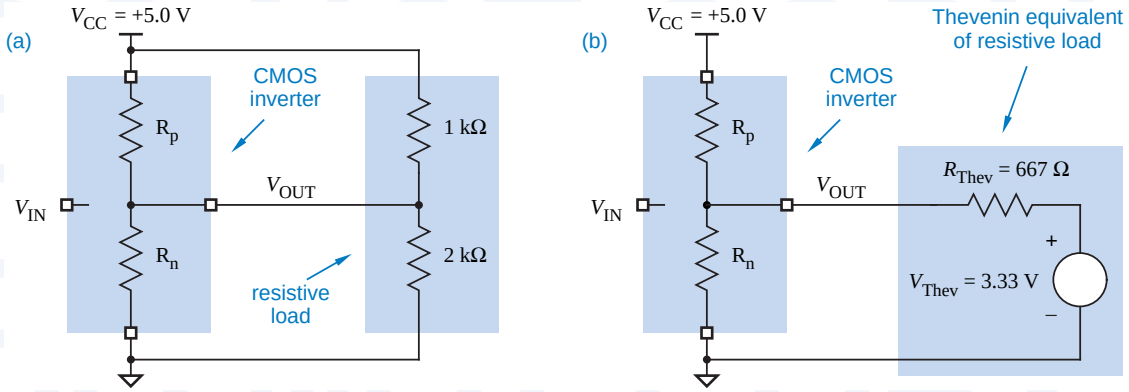


Figure 3-27 Resistive model of a CMOS inverter with a resistive load: (a) showing actual load circuit; (b) using Thévenin equivalent of load.

The input current shown in Table 3-3 for the 'HC00 is only ±1 μA. Thus, it takes very little power to maintain a CMOS input in one state or the other. This is in sharp contrast to bipolar logic circuits like TTL and ECL, whose inputs may consume significant current (and power) in one or both states.

3.5.2 Circuit Behavior with Resistive Loads

resistive load
DC load

As mentioned previously, CMOS gate inputs have very high impedance and consume very little current from the circuits that drive them. There are other devices, however, which require nontrivial amounts of current to operate. When such a device is connected to a CMOS output, we call it a *resistive load* or a *DC load*. Here are some examples of resistive loads:

- Discrete resistors may be included to provide transmission-line termination, discussed in Section 12.4.
- Discrete resistors may not really be present in the circuit, but the load presented by one or more TTL or other non-CMOS inputs may be modeled by a simple resistor network.
- The resistors may be part of or may model a current-consuming device such as a light-emitting diode (LED) or a relay coil.

When the output of a CMOS circuit is connected to a resistive load, the output behavior is not nearly as ideal as we described previously. In either logic state, the CMOS output transistor that is "on" has a nonzero resistance, and a load connected to the output terminal will cause a voltage drop across this resistance. Thus, in the LOW state, the output voltage may be somewhat higher than 0.1 V, and in the HIGH state it may be lower than 4.4 V. The easiest way to see how this happens is look at a resistive model of the CMOS circuit and load.

Copyright © 1999 by John F. Wakerly Copying Prohibited

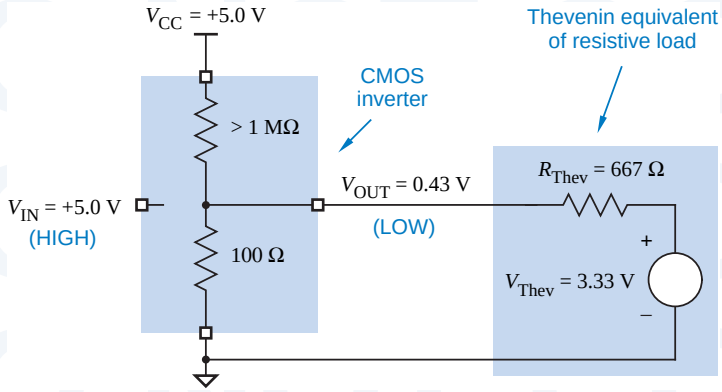


Figure 3-28
Resistive model for CMOS LOW output with resistive load.

Figure 3-27(a) shows the resistive model. The *p*-channel and *n*-channel transistors have resistances R_p and R_n, respectively. In normal operation, one resistance is high (> 1 MΩ) and the other is low (perhaps 100 Ω), depending on whether the input voltage is HIGH or LOW. The load in this circuit consists of two resistors attached to the supply rails; a real circuit may have any resistor values, or an even more complex resistive network. In any case, a resistive load, consisting only of resistors and voltage sources, can always be modeled by a Thévenin equivalent network, such as the one shown in Figure 3-27(b).

When the CMOS inverter has a HIGH input, the output should be LOW; the actual output voltage can be predicted using the resistive model shown in Figure 3-28. The *p*-channel transistor is "off" and has a very high resistance, high enough to be negligible in the calculations that follow. The *n*-channel tran-

REMEMBERING THÉVENIN

Any two-terminal circuit consisting of only voltage sources and resistors can be modeled by a *Thévenin equivalent* consisting of a single voltage source in series with a single resistor. The *Thévenin voltage* is the open-circuit voltage of the original circuit, and the *Thévenin resistance* is the Thévenin voltage divided by the short-circuit current of the original circuit.

In the example of Figure 3-27, the Thévenin voltage of the resistive load, including its connection to V_{CC}, is established by the 1-kΩ and 2-kΩ resistors, which form a voltage divider:

$$V_{Thev} = \frac{2\ \text{k}\Omega}{2\ \text{k}\Omega + 1\text{k}\Omega} \cdot 5.0\ \text{V} = 3.33\ \text{V}$$

The short-circuit current is (5.0 V)/(1 kΩ) = 5 mA, so the Thévenin resistance is (3.33 V)/(5 mA) = 667 Ω. Experienced readers may recognize this as the parallel resistance of the 1-kΩ and 2-Ω resistors.

Copyright © 1999 by John F. Wakerly Copying Prohibited

sistor is "on" and has a low resistance, which we assume to be 100 Ω. (The actual "on" resistance depends on the CMOS family and other characteristics such as operating temperature and whether or not the device was manufactured on a good day.) The "on" transistor and the Thévenin-equivalent resistor R_{Thev} in Figure 3-28 form a simple voltage divider. The resulting output voltage can be calculated as follows:

$$V_{OUT} = 3.33\ V \cdot [100/(100 + 667)]$$
$$= 0.43\ V$$

Similarly, when the inverter has a LOW input, the output should be HIGH, and the actual output voltage can be predicted with the model in Figure 3-29. We'll assume that the *p*-channel transistor's "on" resistance is 200 Ω. Once again, the "on" transistor and the Thévenin-equivalent resistor R_{Thev} in the figure form a simple voltage divider, and the resulting output voltage can be calculated as follows:

$$V_{OUT} = 3.33\ V + (5\ V - 3.33\ V) \cdot [667/(200 + 667)]$$
$$= 4.61\ V$$

In practice, it's seldom necessary to calculate output voltages as in the preceding examples. In fact, IC manufacturers usually don't specify the equivalent resistances of the "on" transistors, so you wouldn't have the necessary information to make the calculation anyway. Instead, IC manufacturers specify a maximum load for the output in each state (HIGH or LOW), and guarantee a worst-case output voltage for that load. The load is specified in terms of current:

I_{OLmax} The maximum current that the output can sink in the LOW state while still maintaining an output voltage no greater than V_{OLmax}.

I_{OHmax} The maximum current that the output can source in the HIGH state while still maintaining an output voltage no less than V_{OHmin}.

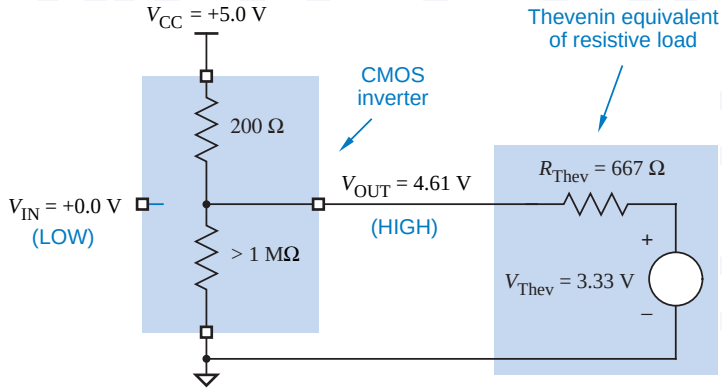


Figure 3-29
Resistive model for CMOS HIGH output with resistive load.

Copyright © 1999 by John F. Wakerly Copying Prohibited

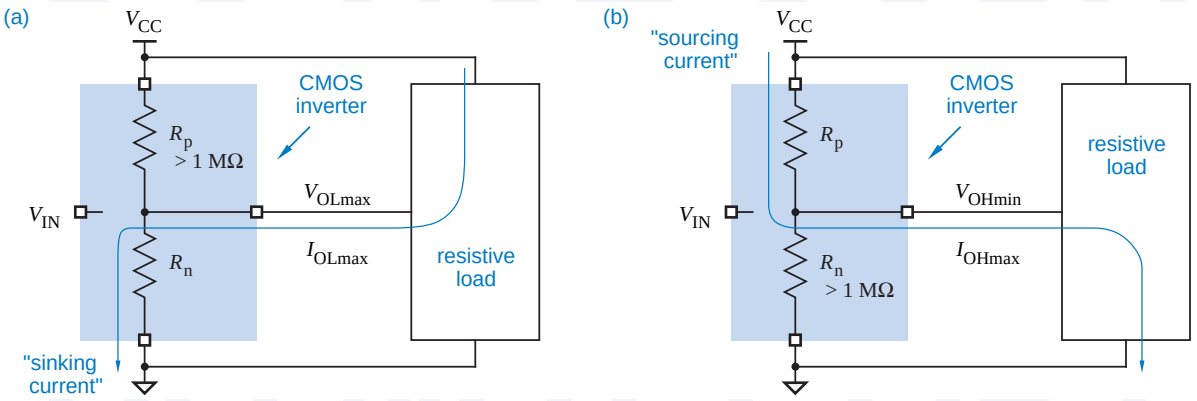


Figure 3-30 Circuit definitions of (a) I_{OLmax}; (b) I_{OHmax}.

These definitions are illustrated in Figure 3-30. A device output is said to *sink current* when current flows from the power supply, through the load, and through the device output to ground as in (a). The output is said to *source current* when current flows from the power supply, out of the device output, and through the load to ground as in (b).

sinking current

sourcing current

Most CMOS devices have two sets of loading specifications. One set is for "CMOS loads," where the device output is connected to other CMOS inputs, which consume very little current. The other set is for "TTL loads," where the output is connected to resistive loads such as TTL inputs or other devices that consume significant current. For example, the specifications for HC-series CMOS outputs were shown in Table 3-3 and are repeated in Table 3-4.

Notice in the table that the output current in the HIGH state is shown as a negative number. By convention, the *current flow* measured at a device terminal is positive if positive current flows *into* the device; in the HIGH state, current flows *out* of the output terminal.

current flow

Table 3-4 Output loading specifications for HC-series CMOS with a 5-volt supply.

	CMOS load		TTL load	
Parameter	**Name**	**Value**	**Name**	**Value**
Maximum LOW-state output current (mA)	I_{OLmaxC}	0.02	I_{OLmaxT}	4.0
Maximum LOW-state output voltage (V)	V_{OLmaxC}	0.1	V_{OLmaxT}	0.33
Maximum HIGH-state output current (mA)	I_{OHmaxC}	–0.02	I_{OHmaxT}	–4.0
Minimum HIGH-state output voltage (V)	V_{OHminC}	4.4	V_{OHminT}	3.84

Copyright © 1999 by John F. Wakerly Copying Prohibited

As the table shows, with CMOS loads, the CMOS gate's output voltage is maintained within 0.1 V of the power-supply rail.With TTL loads, the output voltage may degrade quite a bit. Also notice that for the same output current (±4 mA) the maximum voltage drop with respect to the power-supply rail is twice as much in the HIGH state (0.66 V) as in the LOW state (0.33 V). This suggests that the *p*-channel transistors in HC-series CMOS have a higher "on" resistance than the *n*-channel transistors do. This is natural, since in any CMOS circuit, a *p*-channel transistor has over twice the "on" resistance of an *n*-channel transistor with the same area. Equal voltage drops in both states could be obtained by making the *p*-channel transistors much larger than the *n*-channel transistors, but for various reasons this was not done.

Ohm's law can be used to determine how much current an output sources or sinks in a given situation. In Figure 3-28 on page 99, the "on" *n*-channel transistor modeled by a 100-Ω resistor has a 0.43-V drop across it; therefore it sinks (0.43 V)/(100 Ω) = 4.3 mA of current. Similarly, the "on" *p*-channel transistor in Figure 3-29 sources (0.39 V)/(200 Ω) = 1.95 mA.

The actual "on" resistances of CMOS output transistors usually aren't published, so it's not always possible to use the exact models of the previous paragraphs. However, you can estimate "on" resistances using the following equations, which rely on specifications that are always published:

$$R_{p(on)} = \frac{V_{DD} - V_{OHminT}}{|I_{OHmaxT}|}$$

$$R_{n(on)} = \frac{V_{OLmaxT}}{I_{OLmaxT}}$$

These equations use Ohm's law to compute the "on" resistance as the voltage drop across the "on" transistor divided by the current through it with a worst-case resistive load. Using the numbers given for HC-series CMOS in Table 3-4, we can calculate $R_{p(on)} = 175\ \Omega$ and $R_{n(on)} = 82.5\ \Omega$.

Very good *worst-case* estimates of output current can be made by assuming that there is *no* voltage drop across the "on" transistor. This assumption simplifies the analysis, and yields a conservative result that is almost always good enough for practical purposes. For example, Figure 3-31 shows a CMOS inverter driving the same Thévenin-equivalent load that we've used in previous examples. The resistive model of the output structure is not shown, because it is no longer needed; we assume that there is no voltage drop across the "on" CMOS transistor. In (a), with the output LOW, the entire 3.33-V Thévenin-equivalent voltage source appears across R_{Thev}, and the estimated sink current is (3.33 V)/(667 Ω) = 5.0 mA. In (b), with the output HIGH and assuming a 5.0-V supply, the voltage drop across R_{Thev} is 1.67 V, and the estimated source current is (1.67 V)/(667 Ω) = 2.5 mA.

Copyright © 1999 by John F. Wakerly Copying Prohibited

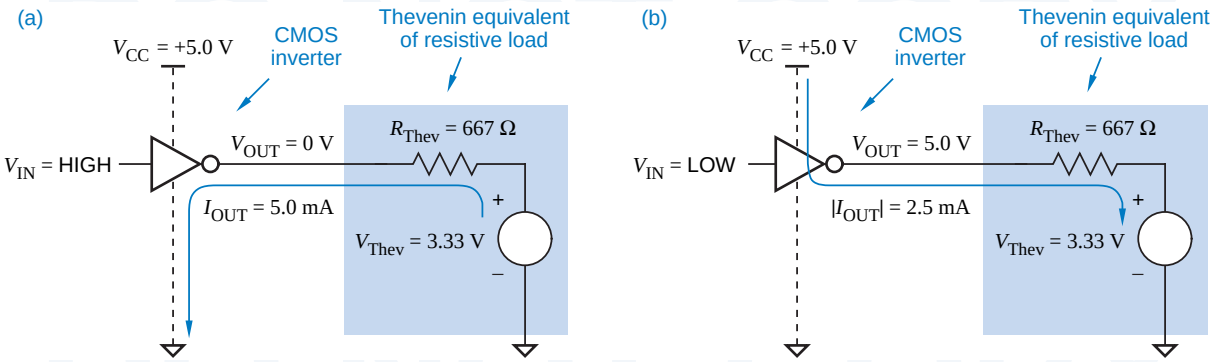


Figure 3-31 Estimating sink and source current: (a) output LOW; (b) output HIGH.

An important feature of the CMOS inverter (or any CMOS circuit) is that the output structure by itself consumes very little current in either state, HIGH or LOW. In either state, one of the transistors is in the high-impedance "off" state. All of the current flow that we've been talking about occurs when a resistive load is connected to the CMOS output. If there's no load, then there's no current flow, and the power consumption is zero. With a load, however, current flows through both the load and the "on" transistor, and power is consumed in both.

THE TRUTH ABOUT POWER CONSUMPTION

As we've stated elsewhere, an "off" transistor's resistance is over one megohm, but it's not infinite. Therefore, a very tiny leakage current actually does flow in "off" transistors and the CMOS output structure does have a correspondingly tiny but non-zero power consumption. In most applications, this power consumption is tiny enough to ignore. It is usually significant only in "standby mode" in battery-powered devices, such as the laptop computer on which this chapter was first prepared.

3.5.3 Circuit Behavior with Nonideal Inputs

So far, we have assumed that the HIGH and LOW inputs to a CMOS circuit are ideal voltages, very close to the power-supply rails. However, the behavior of a real CMOS inverter circuit depends on the input voltage as well as on the characteristics of the load.

If the input voltage is not close to the power-supply rail, then the "on" transistor may not be fully "on" and its resistance may increase. Likewise, the "off" transistor may not be fully "off' and its resistance may be quite a bit less than one megohm. These two effects combine to move the output voltage away from the power-supply rail.

Copyright © 1999 by John F. Wakerly Copying Prohibited

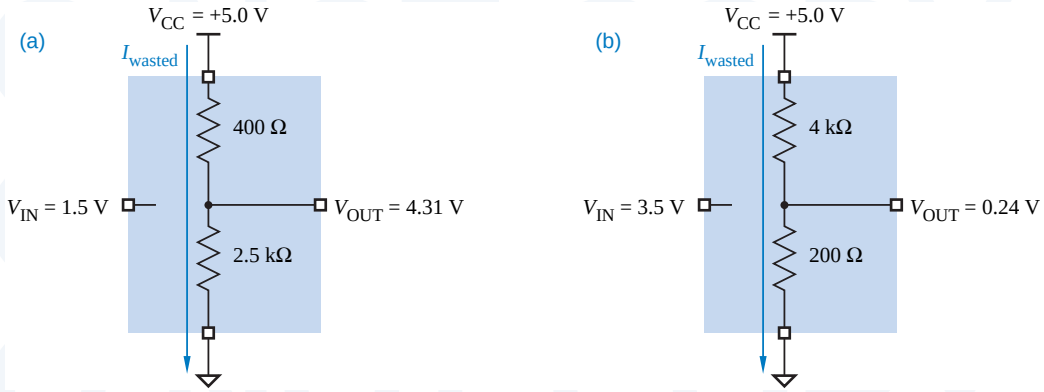


Figure 3-32 CMOS inverter with nonideal input voltages: (a) equivalent circuit with 1.5-V input; (b) equivalent circuit with 3.5-V input.

For example, Figure 3-32(a) shows a CMOS inverter's possible behavior with a 1.5-V input. The *p*-channel transistor's resistance has doubled at this point, and that the *n*-channel transistor is beginning to turn on. (These values are simply assumed for the purposes of illustration; the actual values depend on the detailed characteristics of the transistors.)

In the figure, the output at 4.31 V is still well within the valid range for a HIGH signal, but not quite the ideal of 5.0 V. Similarly, with a 3.5-V input in (b), the LOW output is 0.24 V, not 0 V. The slight degradation of output voltage is generally tolerable; what's worse is that the output structure is now consuming a nontrivial amount of power. The current flow with the 1.5-V input is

$$I_{\text{wasted}} = 5.0\ \text{V}/400\ \Omega + 2.5\ \text{k}\Omega = 1.72\ \text{mA}$$

and the power consumption is

$$P_{\text{wasted}} = 5.0\ \text{V} \cdot I_{\text{wasted}} = 8.62\ \text{mW}$$

The output voltage of a CMOS inverter deteriorates further with a resistive load. Such a load may exist for any of a variety of reasons discussed previously. Figure 3-33 shows a CMOS inverter's possible behavior with a resistive load. With a 1.5-V input, the output at 3.98 V is still within the valid range for a HIGH signal, but it is far from the ideal of 5.0 V. Similarly, with a 3.5-V input as shown in Figure 3-34, the LOW output is 0.93 V, not 0 V.

In "pure" CMOS systems, all of the logic devices in a circuit are CMOS. Since CMOS inputs have a very high impedance, they present very little resistive load to the CMOS outputs that drive them. Therefore, the CMOS output levels all remain very close to the power-supply rails (0 V and 5 V), and none of the devices waste power in their output structures. On the other hand, if TTL outputs or other nonideal logic signals are connected to CMOS inputs, then the CMOS

Copyright © 1999 by John F. Wakerly Copying Prohibited

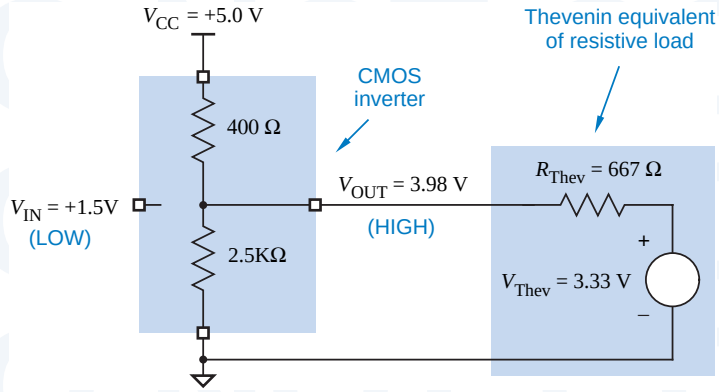


Figure 3-33
CMOS inverter with load and nonideal 1.5-V input.

outputs use power in the way depicted in this subsection; this is formalized in the box at the top of page 135. In addition, if TTL inputs or other resistive loads are connected to CMOS outputs, then the CMOS outputs use power in the way depicted in the preceding subsection.

3.5.4 Fanout

fanout

The *fanout* of a logic gate is the number of inputs that the gate can drive without exceeding its worst-case loading specifications. The fanout depends not only on the characteristics of the output, but also on the inputs that it is driving. Fanout must be examined for both possible output states, HIGH and LOW.

LOW-state fanout

For example, we showed in Table 3-4 on page 101 that the maximum LOW-state output current I_{OLmaxC} for an HC-series CMOS gate driving CMOS inputs is 0.02 mA (20 μA). We also stated previously that the maximum input current I_{Imax} for an HC-series CMOS input in any state is ±1 μA. Therefore, the *LOW-state fanout* for an HC-series output driving HC-series inputs is 20. Table 3-4 also showed that the maximum HIGH-state output current I_{OHmaxC} is

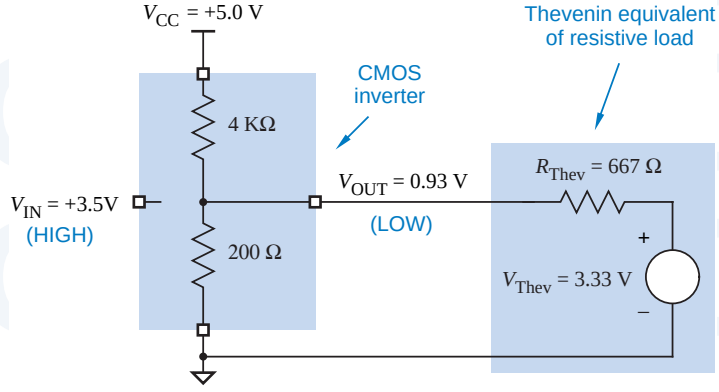


Figure 3-34
CMOS inverter with load and nonideal 3.5-V input.

Copyright © 1999 by John F. Wakerly Copying Prohibited

HIGH-state fanout

–0.02 mA (–20 μA) Therefore, the *HIGH-state fanout* for an HC-series output driving HC-series inputs is also 20.

overall fanout

Note that the HIGH-state and LOW-state fanouts of a gate are not necessarily equal. In general, the *overall fanout* of a gate is the minimum of its HIGH-state and LOW-state fanouts, 20 in the foregoing example.

In the fanout example that we just completed, we assumed that we needed to maintain the gate's output at CMOS levels, that is, within 0.1 V of the power-supply rails. If we were willing to live with somewhat degraded, TTL output levels, then we could use I_{OLmaxT} and I_{OHmaxT} in the fanout calculation. According to Table 3-4, these specifications are 4.0 mA and –4.0 mA, respectively. Therefore, the fanout of an HC-series output driving HC-series inputs at TTL levels is 4000, virtually unlimited, apparently.

DC fanout

Well, not quite. The calculations that we've just carried out give the *DC fanout,* defined as the number of inputs that an output can drive *with the output in a constant state* (HIGH or LOW). Even if the DC fanout specification is met, a CMOS output driving a large number of inputs may not behave satisfactorily on transitions, LOW-to-HIGH or vice versa.

During transitions, the CMOS output must charge or discharge the stray capacitance associated with the inputs that it drives. If this capacitance is too large, the transition from LOW to HIGH (or vice versa) may be too slow, causing improper system operation.

AC fanout

The ability of an output to charge and discharge stray capacitance is sometimes called *AC fanout,* though it is seldom calculated as precisely as DC fanout. As you'll see in Section 3.6.1, it's more a matter of deciding how much speed degradation you're willing to live with.

3.5.5 Effects of Loading

Loading an output beyond its rated fanout has several effects:

- In the LOW state, the output voltage (V_{OL}) may increase beyond V_{OLmax}.
- In the HIGH state, the output voltage (V_{OH}) may fall below V_{OHmin}.
- Propagation delay to the output may increase beyond specifications.
- Output rise and fall times may increase beyond their specifications.
- The operating temperature of the device may increase, thereby reducing the reliability of the device and eventually causing device failure.

The first four effects reduce the DC noise margins and timing margins of the circuit. Thus, a slightly overloaded circuit may work properly in ideal conditions, but experience says that it will fail once it's out of the friendly environment of the engineering lab.

Copyright © 1999 by John F. Wakerly Copying Prohibited

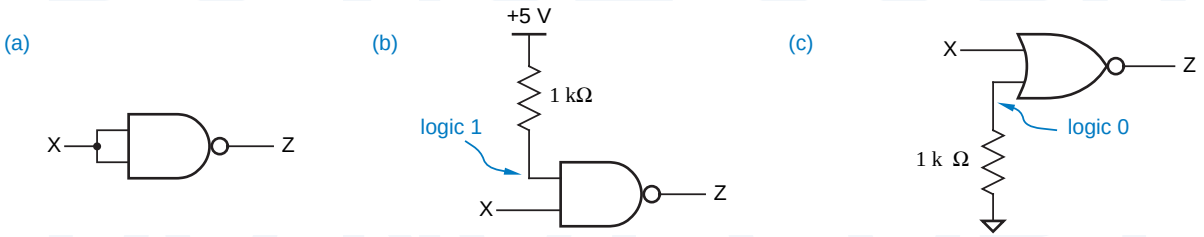


Figure 3-35 Unused inputs: (a) tied to another input; (b) NAND pulled up; (c) NOR pulled down.

3.5.6 Unused Inputs

Sometimes not all of the inputs of a logic gate are used. In a real design problem, you may need an n-input gate but have only an n+1-input gate available. Tying together two inputs of the n+1-input gate gives it the functionality of an n-input gate. You can convince yourself of this fact intuitively now, or use switching algebra to prove it after you've studied Section 4.1. Figure 3-35(a) shows a NAND gate with its inputs tied together.

You can also tie unused inputs to a constant logic value. An unused AND or NAND input should be tied to logic 1, as in (b), and an unused OR or NOR input should be tied to logic 0, as in (c). In high-speed circuit design, it's usually better to use method (b) or (c) rather than (a), which increases the capacitive load on the driving signal and may slow things down. In (b) and (c), a resistor value in the range 1–10 kΩ is typically used, and a single pull-up or pull-down resistor can serve multiple unused inputs. It is also possible to tie unused inputs directly to the appropriate power-supply rail.

floating input

Unused CMOS inputs should never be left unconnected (or *floating*. On one hand, such an input will behave as if it had a LOW signal applied to it and will normally show a value of 0 V when probed with an oscilloscope or voltmeter. So you might think that an unused OR or NOR input can be left floating, because it will act as if a logic 0 is applied and not affect the gate's output. How-

SUBTLE BUGS Floating CMOS inputs are often the cause of mysterious circuit behavior, as an unused input erratically changes its effective state based on noise and conditions elsewhere in the circuit. When you're trying to debug such a problem, the extra capacitance of an oscilloscope probe touched to the floating input is often enough to damp out the noise and make the problem go away. This can be especially baffling if you don't realize that the input is floating!

Copyright © 1999 by John F. Wakerly Copying Prohibited

ever, since CMOS inputs have such high impedance, it takes only a small amount of circuit noise to temporarily make a floating input look HIGH, creating some very nasty intermittent circuit failures.

3.5.7 Current Spikes and Decoupling Capacitors

current spikes

When a CMOS output switches between LOW and HIGH, current flows from V_{CC} to ground through the partially-on *p*- and *n*-channel transistors. These currents, often called *current spikes* because of their brief duration, may show up as noise on the power-supply and ground connections in a CMOS circuit, especially when multiple outputs are switched simultaneously.

decoupling capacitors

filtering capacitors

For this reason, systems that use CMOS circuits require *decoupling capacitors* between V_{CC} and ground. These capacitors must be distributed throughout the circuit, at least one within an inch or so of each chip, to supply current during transitions. The large *filtering capacitors* typically found in the power supply itself don't satisfy this requirement, because stray wiring inductance prevents them from supplying the current fast enough, hence the need for a *physically distributed* system of decoupling capacitors.

3.5.8 How to Destroy a CMOS Device

Hit it with a sledge hammer. Or simply walk across a carpet and then touch an input pin with your finger. Because CMOS device inputs have such high impedance, they are subject to damage from *electrostatic discharge (ESD)*.

electrostatic discharge (ESD)

ESD occurs when a buildup of charge on one surface arcs through a dielectric to another surface with the opposite charge. In the case of a CMOS input, the dielectric is the insulation between an input transistor's gate and its source and drain. ESD may damage this insulation, causing a short-circuit between the device's input and output.

The input structures of modern CMOS devices use various measures to reduce their susceptibility to ESD damage, but no device is completely immune. Therefore, to protect CMOS devices from ESD damage during shipment and handling, manufacturers normally package their devices in conductive bags, tubes, or foam. To prevent ESD damage when handling loose CMOS devices, circuit assemblers and technicians usually wear conductive wrist straps that are connected by a coil cord to earth ground; this prevents a static charge from building up on their bodies as they move around the factory or lab.

latch-up

Once a CMOS device is installed in a system, another possible source of damage is *latch-up*. The physical input structure of just about any CMOS device contains parasitic bipolar transistors between V_{CC} and ground configured as a silicon-controlled rectifier (SCR)." In normal operation, this "parasitic SCR" has no effect on device operation. However, an input voltage that is less than ground or more than V_{CC} can "trigger" the SCR, creating a virtual short-circuit between V_{CC} and ground. Once the SCR is triggered, the only way to turn it off

Copyright © 1999 by John F. Wakerly Copying Prohibited

ELIMINATE RUDE, SHOCKING BEHAVIOR!

Some design engineers consider themselves above such inconveniences, but to be safe you should follow several ESD precautions in the lab:

- Before handling a CMOS device, touch the grounded metal case of a plugged-in instrument or another source of earth ground.
- Before transporting a CMOS device, insert it in conductive foam.
- When carrying a circuit board containing CMOS devices, handle the board by the edges, and touch a ground terminal on the board to earth ground before poking around with it.
- When handing over a CMOS device to a partner, especially on a dry winter day, touch the partner first. He or she will thank you for it.

is to turn off the power supply. Before you have a chance to do this, enough power may be dissipated to destroy the device (i.e., you may see smoke).

One possible trigger for latch-up is "undershoot" on high-speed HIGH-to-LOW signal transitions, discussed in Section 12.4. In this situation, the input signal may go several volts below ground for several nanoseconds before settling into the normal LOW range. However, modern CMOS logic circuits are fabricated with special structures that prevent latch-up in this transient case.

Latch-up can also occur when CMOS inputs are driven by the outputs of another system or subsystem with a separate power supply. If a HIGH input is applied to a CMOS gate before power is present, the gate may come up in the "latched-up" state when power is applied. Again, modern CMOS logic circuits are fabricated with special structures that prevent this in most cases. However, if the driving output is capable of sourcing lots of current (e.g., tens of mA), latch-up is still possible. One solution to this problem is to apply power before hooking up input cables.

3.6 CMOS Dynamic Electrical Behavior

Both the speed and the power consumption of a CMOS device depend to a large extent on AC or dynamic characteristics of the device and its load, that is, what happens when the output changes between states. As part of the internal design of CMOS ASICs, logic designers must carefully examine the effects of output loading and redesign where the load is too high. Even in board-level design, the effects of loading must be considered for clocks, buses, and other signals that have high fanout or long interconnections.

Speed depends on two characteristics, transition time and propagation delay, discussed in the next two subsections. Power dissipation is discussed in the third subsection.

Copyright © 1999 by John F. Wakerly Copying Prohibited

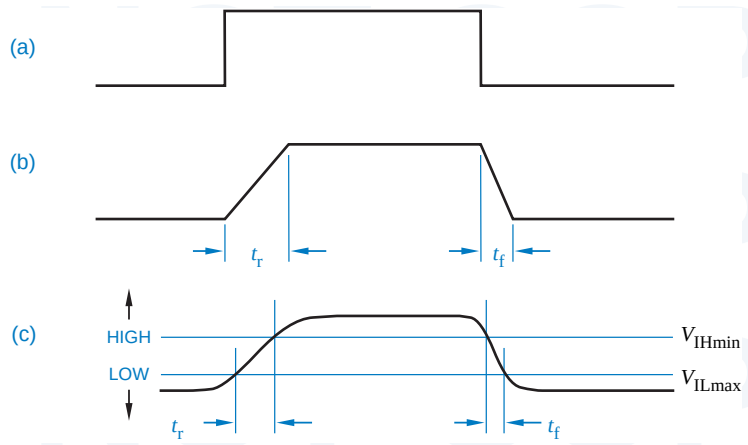


Figure 3-36
Transition times: (a) ideal case of zero-time switching; (b) a more realistic approximation; (c) actual timing, showing rise and fall times.

3.6.1 Transition Time

transition time

The amount of time that the output of a logic circuit takes to change from one state to another is called the *transition time*. Figure 3-36(a) shows how we might like outputs to change state—in zero time. However, real outputs cannot change instantaneously, because they need time to charge the stray capacitance of the wires and other components that they drive. A more realistic view of a circuit's output is shown in (b). An output takes a certain time, called the *rise time* (t_r), to change from LOW to HIGH, and a possibly different time, called the *fall time* (t_f), to change from HIGH to LOW.

rise time (t_r)
fall time (t_f)

Even Figure 3-36(b) is not quite accurate, because the rate of change of the output voltage does not change instantaneously, either. Instead, the beginning and the end of a transition are smooth, as shown in (c). To avoid difficulties in defining the endpoints, rise and fall times are normally measured at the boundaries of the valid logic levels as indicated in the figure.

With the convention in (c), the rise and fall times indicate how long an output voltage takes to pass through the "undefined" region between LOW and HIGH. The initial part of a transition is not included in the rise- or fall-time number. Instead, the initial part of a transition contributes to the "propagation delay" number discussed in the next subsection.

The rise and fall times of a CMOS output depend mainly on two factors, the "on" transistor resistance and the load capacitance. A large capacitance increases transition times; since this is undesirable, it is very rare for a logic designer to purposely connect a capacitor to a logic circuit's output. However, *stray capacitance* is present in every circuit; it comes from at least three sources:

stray capacitance

1. Output circuits, including a gate's output transistors, internal wiring, and packaging, have some capacitance associated with them, on the order of 2–10 picofarads (pF) in typical logic families, including CMOS.

Copyright © 1999 by John F. Wakerly Copying Prohibited

2. The wiring that connects an output to other inputs has capacitance, about 1 pF per inch or more, depending on the wiring technology.
3. Input circuits, including transistors, internal wiring, and packaging, have capacitance, from 2 to 15 pF per input in typical logic families.

Stray capacitance is sometimes called a *capacitive load* or an *AC load*. *capacitive load* *AC load*

A CMOS output's rise and fall times can be analyzed using the equivalent circuit shown in Figure 3-37. As in the preceding section, the *p*-channel and *n*-channel transistors are modeled by resistances R_p and R_n, respectively. In normal operation, one resistance is high and the other is low, depending on the output's state. The output's load is modeled by an *equivalent load circuit* with three components: *equivalent load circuit*

R_L, V_L These two components represent the DC load and determine the voltages and currents that are present when the output has settled into a stable HIGH or LOW state. The DC load doesn't have too much effect on transition times when the output changes states.

C_L This capacitance represents the AC load and determines the voltages and currents that are present while the output is changing, and how long it takes to change from one state to the other

When a CMOS output drives only CMOS inputs, the DC load is negligible. To simplify matters, we'll analyze only this case, with $R_L = \infty$ and $V_L = 0$, in the remainder of this subsection. The presence of a nonnegligible DC load would affect the results, but not dramatically (see Exercise 3.69).

We can now analyze the transition times of a CMOS output. For the purposes of this analysis, we'll assume C_L= 100 pF, a moderate capacitive load. Also, we'll assume that the "on" resistances of the *p*-channel and *n*-channel transistors are 200 Ω and 100 Ω, respectively, as in the preceding subsection. The rise and fall times depend on how long it takes to charge or discharge the capacitive load C_L.

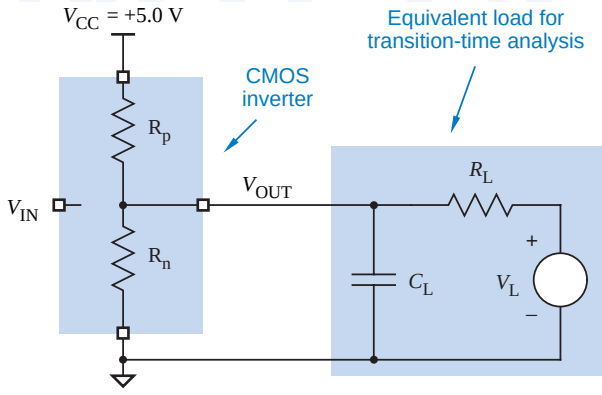


Figure 3-37
Equivalent circuit for analyzing transition times of a CMOS output.

Copyright © 1999 by John F. Wakerly Copying Prohibited

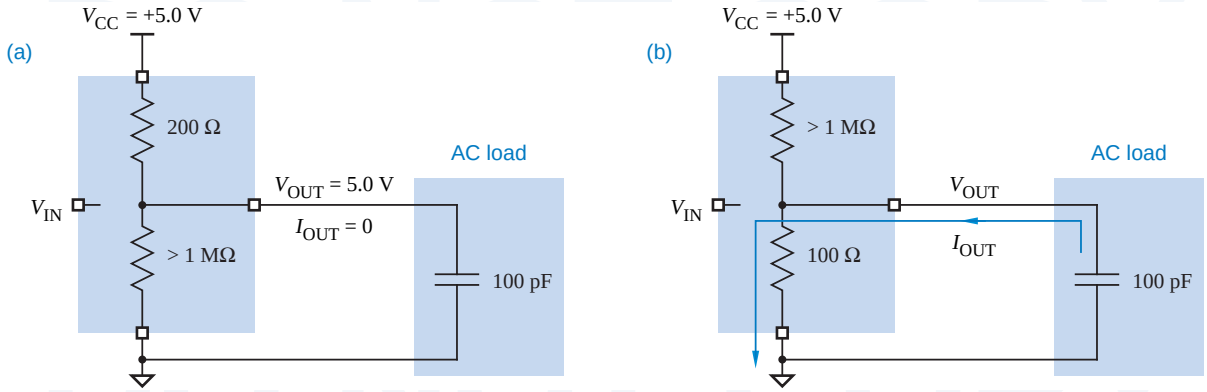


Figure 3-38 Model of a CMOS HIGH-to-LOW transition: (a) in the HIGH state; (b) after *p*-channel transistor turns off and *n*-channel transistor turns on.

First, we'll look at fall time. Figure 3-38(a) shows the electrical conditions in the circuit when the output is in a steady HIGH state. (R_L and V_L are not drawn; they have no effect, since we assume $R_L = \infty$.) For the purposes of our analysis, we'll assume that when CMOS transistors change between "on" and "off," they do so instantaneously. We'll assume that at time $t = 0$ the CMOS output changes to the LOW state, resulting in the situation depicted in (b).

At time $t = 0$, V_{OUT} is still 5.0 V. (A useful electrical engineering maxim is that the voltage across a capacitor cannot change instantaneously.) At time $t = \infty$, the capacitor must be fully discharged and V_{OUT} will be 0 V. In between, the value of V_{OUT} is governed by an exponential law:

$$\begin{aligned} V_{OUT} &= V_{DD} \cdot e^{-t/R_n C_L} \\ &= 5.0 \cdot e^{-t(100 \cdot 100 \cdot 10^{-12})} \\ &= 5.0 \cdot e^{-t/(10 \cdot 10^{-9})} \text{ V} \end{aligned}$$

RC time constant

The factor $R_n C_L$ has units of seconds, and is called an *RC time constant*. The preceding calculation shows that the *RC* time constant for HIGH-to-LOW transitions is 10 nanoseconds (ns).

Figure 3-39 plots V_{OUT} as a function of time. To calculate fall time, recall that 1.5 V and 3.5 V are the defined boundaries for LOW and HIGH levels for CMOS inputs being driven by the CMOS output. To obtain the fall time, we must solve the preceding equation for $V_{OUT} = 3.5$ and $V_{OUT} = 1.5$, yielding:

$$t = -R_n C_L \cdot \ln\frac{V_{OUT}}{V_{DD}} = -10 \cdot 10^{-9} \cdot \ln\frac{V_{OUT}}{5.0}$$

$$t_{3.5} = 3.57 \text{ ns}$$

$$t_{1.5} = 12.04 \text{ ns}$$

Copyright © 1999 by John F. Wakerly Copying Prohibited

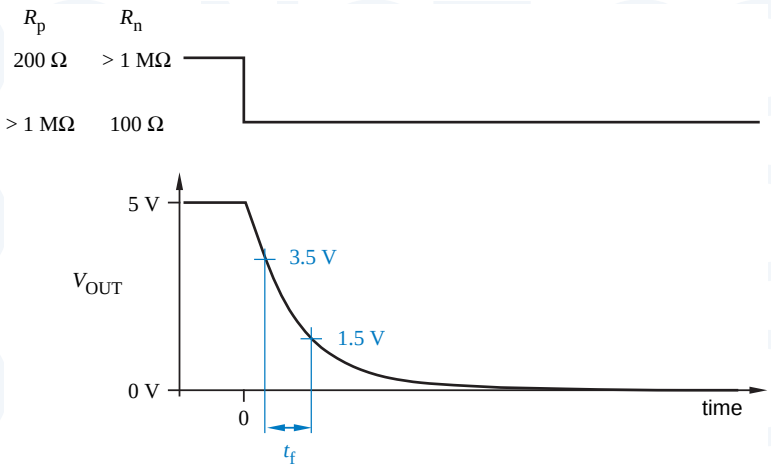


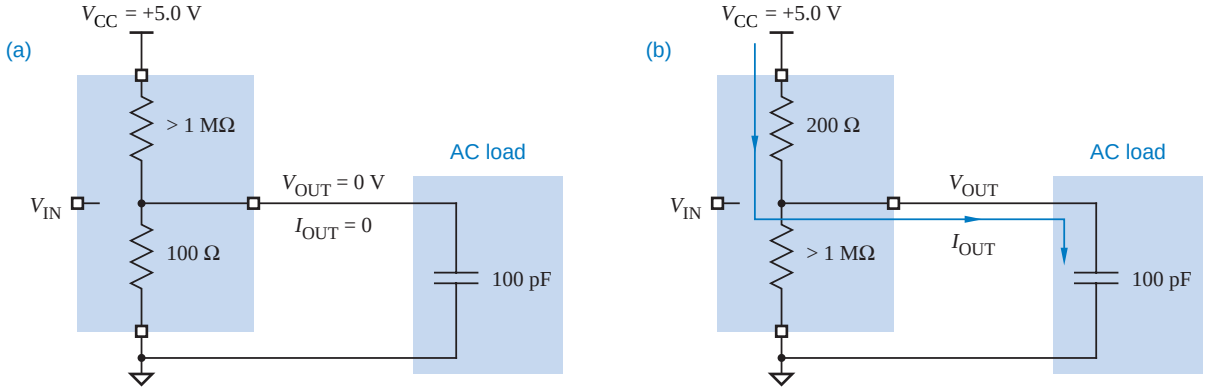
Figure 3-39 Fall time for a HIGH-to-LOW transition of a CMOS output.

The fall time t_f is the difference between these two numbers, or about 8.5 ns.

Rise time can be calculated in a similar manner. Figure 3-40(a) shows the conditions in the circuit when the output is in a steady LOW state. If at time $t = 0$ the CMOS output changes to the HIGH state, the situation depicted in (b) results. Once again, V_{OUT} cannot change instantly, but at time $t = \infty$, the capacitor will be fully charged and V_{OUT} will be 5.0 V. Once again, the value of V_{OUT} in between is governed by an exponential law:

$$\begin{aligned} V_{OUT} &= V_{DD} \cdot (1 - e^{-t/R_p C_L}) \\ &= 5.0 \cdot (1 - e^{-t(200 \cdot 100 \cdot 10^{-12})}) \\ &= 5.0 \cdot (1 - e^{-t/(20 \cdot 10^{-9})}) \text{ V} \end{aligned}$$

Figure 3-40 Model of a CMOS LOW-to-HIGH transition: (a) in the LOW state; (b) after *n*-channel transistor turns off and *p*-channel transistor turns on.



Copyright © 1999 by John F. Wakerly Copying Prohibited

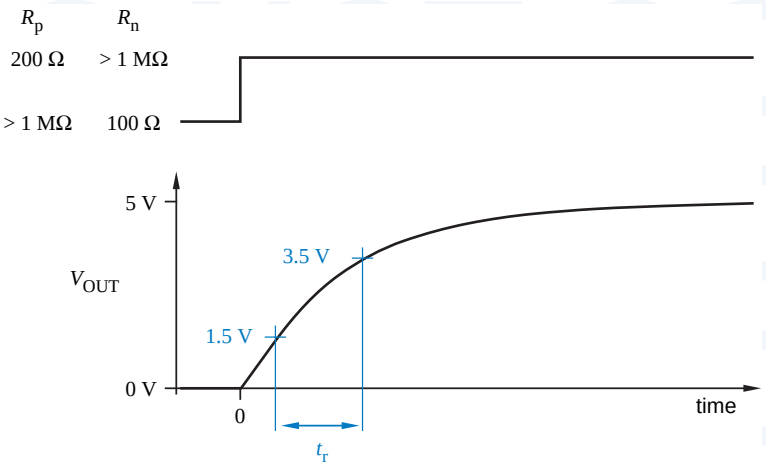


Figure 3-41
Rise time for a LOW-to-HIGH transition of a CMOS output.

The *RC* time constant in this case is 20 ns. Figure 3-41 plots V_{OUT} as a function of time. To obtain the rise time, we must solve the preceding equation for $V_{OUT} = 1.5$ and $V_{OUT} = 3.5$, yielding

$$t = -RC \cdot \ln\frac{V_{DD} - V_{OUT}}{V_{DD}}$$

$$= -20 \cdot 10^{-9} \cdot \ln\frac{5.0 - V_{OUT}}{5.0}$$

$$t_{1.5} = 7.13 \text{ ns}$$

$$t_{3.5} = 24.08 \text{ ns}$$

The rise time t_r is the difference between these two numbers, or about 17 ns.

The foregoing example assumes that the *p*-channel transistor has twice the resistance of the *n*-channel one, and as a result the rise time is twice as long as the fall time. It takes longer for the "weak" *p*-channel transistor to pull the output up than it does for the "strong" *n*-channel transistor to pull it down; the output's drive capability is "asymmetric." High-speed CMOS devices are sometimes fabricated with larger *p*-channel transistors to make the transition times more nearly equal and output drive more symmetric.

Regardless of the transistors' characteristics, an increase in the load capacitance cause an increase in the *RC* time constant, and a corresponding increase in the transition times of the output. Thus, it is a goal of high-speed circuit designers to minimize load capacitance, especially on the most timing-critical signals. This can be done by minimizing the number of inputs driven by the signal, by creating multiple copies of the signal, and by careful physical layout of the circuit.

Copyright © 1999 by John F. Wakerly Copying Prohibited

When working with real digital circuits, it's often useful to estimate transition times, without going through a detailed analysis. A useful rule of thumb is that the transition time approximately equals the *RC* time constant of the charging or discharging circuit. For example, estimates of 10 and 20 ns for fall and rise time in the preceding example would have been pretty much on target, especially considering that most assumptions about load capacitance and transistor "on" resistances are approximate to begin with.

Manufacturers of commercial CMOS circuits typically do not specify transistor "on" resistances on their data sheets. If you search carefully, you might find this information published in the manufacturers' application notes. In any case, you can estimate an "on" resistance as the voltage drop across the "on" transistor divided by the current through it with a worst-case resistive load, as we showed in Section 3.5.2:

$$R_{p(on)} = \frac{V_{DD} - V_{OHminT}}{|I_{OHmaxT}|}$$

$$R_{n(on)} = \frac{V_{OLmaxT}}{|I_{OLmaxT}|}$$

THERE'S A CATCH!

Calculated transition times are actually quite sensitive to the choice of logic levels. In the examples in this subsection, if we used 2.0 V and 3.0 V instead of 1.5 V and 3.5 V as the thresholds for LOW and HIGH, we would calculate shorter transition times. On the other hand, if we used 0.0 and 5.0 V, the calculated transition times would be infinity! You should also be aware that in some logic families (most notably TTL), the thresholds are not symmetric around the voltage midpoint. Still, it is the author's experience that the "time-constant-equals-transition-time" rule of thumb usually works for practical circuits.

3.6.2 Propagation Delay

Rise and fall times only partially describe the dynamic behavior of a logic element; we need additional parameters to relate output timing to input timing. A *signal path* is the electrical path from a particular input signal to a particular output signal of a logic element. The *propagation delay* t_p of a signal path is the amount of time that it takes for a change in the input signal to produce a change in the output signal.

signal path
propagation delay t_p

A complex logic element with multiple inputs and outputs may specify a different value of t_p for each different signal path. Also, different values may be specified for a particular signal path, depending on the direction of the output change. Ignoring rise and fall times, Figure 3-42(a) shows two different propa-

Copyright © 1999 by John F. Wakerly Copying Prohibited

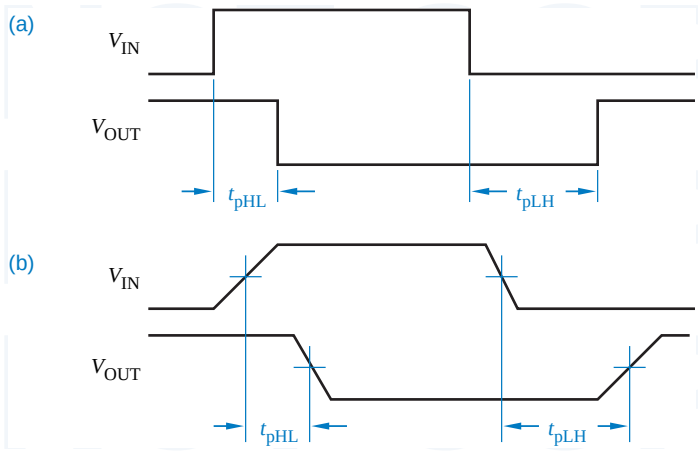


Figure 3-42
Propagation delays for a CMOS inverter: (a) ignoring rise and fall times; (b) measured at midpoints of transitions.

gation delays for the input-to-output signal path of a CMOS inverter, depending on the direction of the output change:

t_{pHL}

t_{pHL} The time between an input change and the corresponding output change when the output is changing from HIGH to LOW.

t_{pLH}

t_{pLH} The time between an input change and the corresponding output change when the output is changing from LOW to HIGH.

Several factors lead to nonzero propagation delays. In a CMOS device, the rate at which transistors change state is influenced both by the semiconductor physics of the device and by the circuit environment, including input-signal transition rate, input capacitance, and output loading. Multistage devices such as noninverting gates or more complex logic functions may require several internal transistors to change state before the output can change state. And even when the output begins to change state, with nonzero rise and fall times it takes quite some time to cross the region between states, as we showed in the preceding subsection. All of these factors are included in propagation delay.

To factor out the effect of rise and fall times, manufacturers usually specify propagation delays at the midpoints of input and output transitions, as shown in Figure 3-42(b). However, sometimes the delays are specified at the logic-level boundary points, especially if the device's operation may be adversely affected by slow rise and fall times. For example, Figure 3-43 shows how the minimum input pulse width for an SR latch (discussed in Section 7.2.1) might be specified.

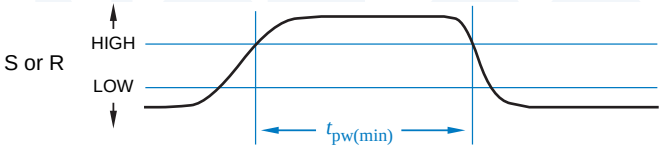


Figure 3-43
Worst-case timing specified using logic-level boundary points.

Copyright © 1999 by John F. Wakerly Copying Prohibited

In addition, a manufacturer may specify absolute maximum input rise and fall times that must be satisfied to guarantee proper operation. High-speed CMOS circuits may consume excessive current or oscillate if their input transitions are too slow.

3.6.3 Power Consumption

The power consumption of a CMOS circuit whose output is not changing is called *static power dissipation* or *quiescent power dissipation*. (The words *consumption* and *dissipation* are used pretty much interchangeably when discussing how much power a device uses.) Most CMOS circuits have very low static power dissipation. This is what makes them so attractive for laptop computers and other low-power applications—when computation pauses, very little power is consumed. A CMOS circuit consumes significant power only during transitions; this is called *dynamic power dissipation*.

static power dissipation

quiescent power dissipation

dynamic power dissipation

One source of dynamic power dissipation is the partial short-circuiting of the CMOS output structure. When the input voltage is not close to one of the power supply rails (0 V or V_{CC}), both the *p*-channel and *n*-channel output transistors may be partially "on," creating a series resistance of 600 Ω or less. In this case, current flows through the transistors from V_{CC} to ground. The amount of power consumed in this way depends on both the value of V_{CC} and the rate at which output transitions occur, according to the formula

$$P_T = C_{PD} \cdot V_{CC}^2 \cdot f$$

The following variables are used in the formula:

P_T The circuit's internal power dissipation due to output transitions.

V_{CC} The power supply voltage. As all electrical engineers know, power dissipation across a resistive load (the partially-on transistors) is proportional to the *square* of the voltage.

f The *transition frequency* of the output signal. This specifies the number of power-consuming output transitions per second. (But note that frequency is defined as the number of transitions divided by 2.)

transition frequency

C_{PD} The *power dissipation capacitance*. This constant, normally specified by the device manufacturer, completes the formula. C_{PD} turns out to have units of capacitance, but does not represent an actual output capacitance. Rather, it embodies the dynamics of current flow through the changing output-transistor resistances during a single pair of output transitions, HIGH-to-LOW and LOW-to-HIGH. For example, C_{PD} for HC-series CMOS gates is typically 20–24 pF, even though the actual output capacitance is much less.

power dissipation capacitance

The P_T formula is valid only if input transitions are fast enough, leading to fast output transitions. If the input transitions are too slow, then the output

Copyright © 1999 by John F. Wakerly Copying Prohibited

transistors stay partially on for a longer time, and power consumption increases. Device manufacturers usually recommend a maximum input rise and fall time, below which the value specified for C_{PD} is valid.

A second, and often more significant, source of CMOS power consumption is the capacitive load (C_L) on the output. During a LOW-to-HIGH transition, current flows through a *p*-channel transistor to charge C_L. Likewise, during a HIGH-to-LOW transition, current flows through an *n*-channel transistor to discharge C_L. In each case, power is dissipated in the "on" resistance of the transistor. We'll use P_L to denote the total amount of power dissipated by charging and discharging C_L.

The units of P_L are power, or energy usage per unit time. The energy for one transition could be determined by calculating the current through the charging transistor as a function of time (using the *R*C time constant as in Section 3.6.1), squaring this function, multiplying by the "on" resistance of the charging transistor, and integrating over time. An easier way is described below.

During a transition, the voltage across the load capacitance C_L changes by $\pm V_{CC}$. According to the definition of capacitance, the total amount of charge that must flow to make a voltage change of V_{CC} across C_L is $C_L \cdot V_{CC}$. The total amount of energy used in one transition is charge times the average voltage change. The first little bit of charge makes a voltage change of V_{CC}, while the last bit of charge makes a vanishingly small voltage change, hence the average change is $V_{CC}/2$. The total energy per transition is therefore $C_L \cdot V_{CC}^2/2$. If there are $2f$ transitions per second, the total power dissipated due to the capacitive load is

$$\begin{aligned} P_L &= C_L \cdot (V_{CC}^2/2) \cdot 2f \\ &= C_L \cdot V_{CC}^2 \cdot f \end{aligned}$$

The total dynamic power dissipation of a CMOS circuit is the sum of P_T and P_L:

$$\begin{aligned} P_D &= P_T + P_L \\ &= C_{PD} \cdot V_{CC}^2 \cdot f + C_L \cdot V_{CC}^2 \cdot f \\ &= (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f \end{aligned}$$

CV^2f power

Based on this formula, dynamic power dissipation is often called *CV^2f power*. In most applications of CMOS circuits, CV^2f power is by far the major contributor to total power dissipation. Note that CV^2f power is also consumed by bipolar logic circuits like TTL and ECL, but at low to moderate frequencies it is insignificant compared to the static (DC or quiescent) power dissipation of bipolar circuits.

Copyright © 1999 by John F. Wakerly Copying Prohibited

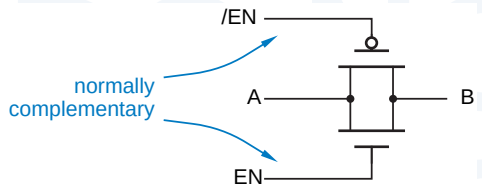


Figure 3-44
CMOS transmission gate.

3.7 Other CMOS Input and Output Structures

Circuit designers have modified the basic CMOS circuit in many ways to produce gates that are tailored for specific applications. This section describes some of the more common variations in CMOS input and output structures.

3.7.1 Transmission Gates

A *p*-channel and *n*-channel transistor pair can be connected together to form a logic-controlled switch. Shown in Figure 3-44(a), this circuit is called a CMOS *transmission gate*.

transmission gate

A transmission gate is operated so that its input signals EN and /EN are always at opposite levels. When EN is HIGH and /EN is LOW, there is a low-impedance connection (as low as 2–5 Ω) between points A and B. When EN is LOW and /EN is HIGH, points A and B are disconnected.

Once a transmission gate is enabled, the propagation delay from A to B (or vice versa) is very short. Because of their short delays and conceptual simplicity, transmission gates are often used internally in larger-scale CMOS devices such as multiplexers and flip-flops. For example, Figure 3-45 shows how transmission gates can be used to create a "2-input multiplexer." When S is LOW, the X "input" is connected to the Z "output"; when S is HIGH, Y is connected to Z.

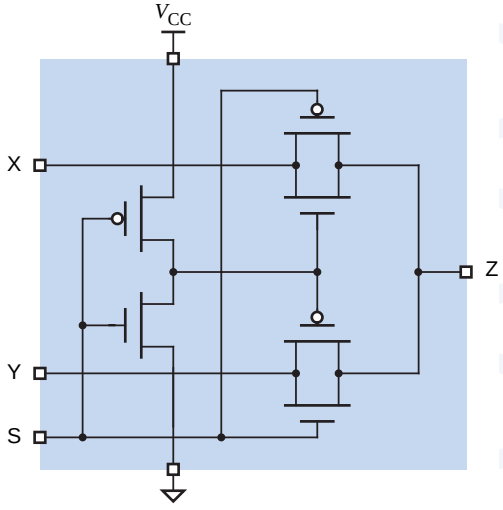


Figure 3-45
Two-input multiplexer using CMOS transmission gates.

Copyright © 1999 by John F. Wakerly Copying Prohibited

At least one commercial manufacturer (Quality Semiconductor) makes a variety of logic functions based on transmission gates. In their multiplexer devices, it takes several nanoseconds for a change in the "select" inputs (such as in Figure 3-45) to affect the input-output path (X or Y to Z). Once a path is set up, however, the propagation delay from input to output is specified to be at most 0.25 ns; this is the fastest discrete CMOS multiplexer you can buy.

3.7.2 Schmitt-Trigger Inputs

Schmitt-trigger input

The input-output transfer characteristic for a typical CMOS gate was shown in Figure 3-25 on page 96. The corresponding transfer characteristic for a gate with *Schmitt-trigger inputs* is shown in Figure 3-46(a). A Schmitt trigger is a special circuit that uses feedback internally to shift the switching threshold depending on whether the input is changing from LOW to HIGH or from HIGH to LOW.

For example, suppose the input of a Schmitt-trigger inverter is initially at 0 V, a solid LOW. Then the output is HIGH, close to 5.0 V. If the input voltage is increased, the output will not go LOW until the input voltage reaches about 2.9 V. However, once the output is LOW, it will not go HIGH again until the input is decreased to about 2.1 V. Thus, the switching threshold for positive-going input changes, denoted V_{T+}, is about 2.9 V, and for negative-going input changes, denoted V_{T-}, is about 2.1 V. The difference between the two thresholds is called *hysteresis*. The Schmitt-trigger inverter provides about 0.8 V of hysteresis.

hysteresis

To demonstrate the usefulness of hysteresis, Figure 3-47(a) shows an input signal with long rise and fall times and about 0.5 V of noise on it. An ordinary inverter, without hysteresis, has the same switching threshold for both positive-going and negative-going transitions, $V_T \approx 2.5$ V. Thus, the ordinary inverter responds to the noise as shown in (b), producing multiple output changes each time the noisy input voltage crosses the switching threshold. However, as shown in (c), a Schmitt-trigger inverter does not respond to the noise, because its hysteresis is greater than the noise amplitude.

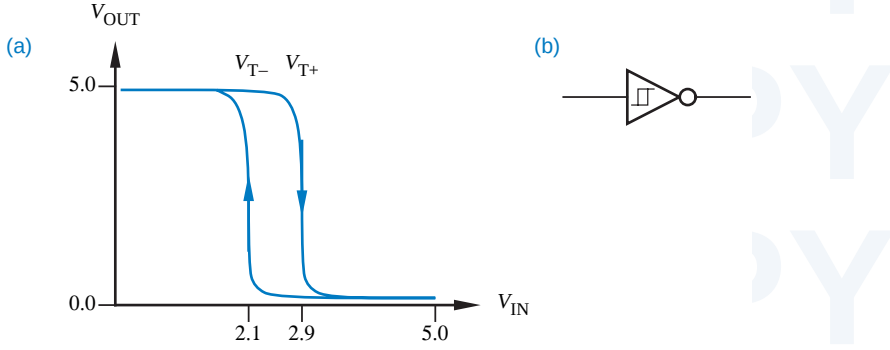


Figure 3-46
A Schmitt-trigger inverter: (a) input-output transfer characteristic; (b) logic symbol.

Copyright © 1999 by John F. Wakerly Copying Prohibited

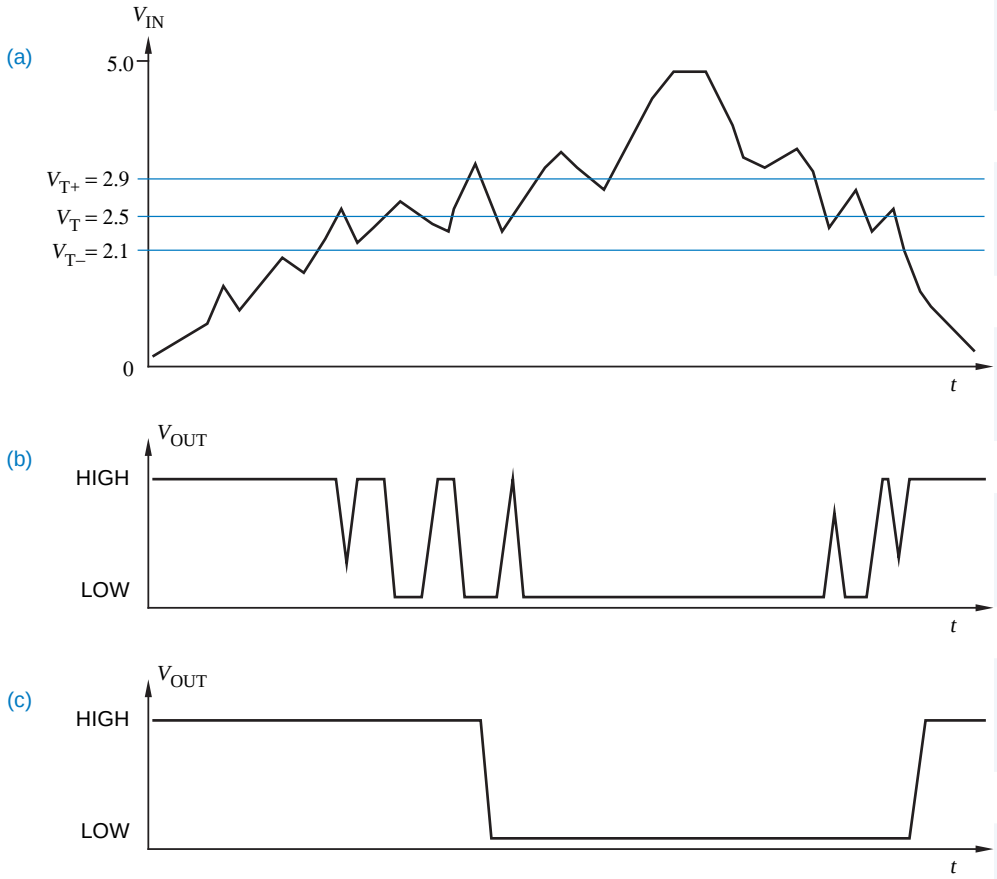
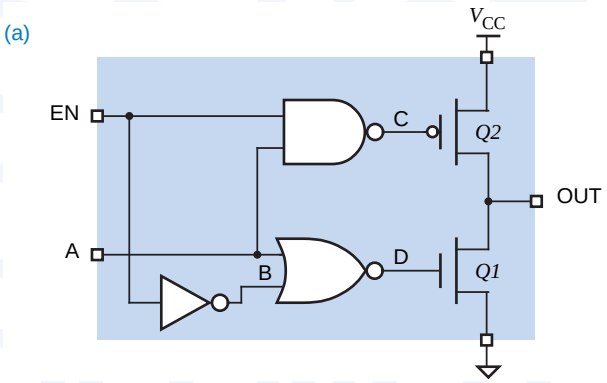


Figure 3-47 Device operation with slowly changing inputs: (a) a noisy, slowly changing input; (b) output produced by an ordinary inverter; (c) output produced by an inverter with 0.8 V of hysteresis.

FIXING YOUR TRANSMISSION

Schmitt-trigger inputs have better noise immunity than ordinary gate inputs for signals that contain transmission-line reflections, discussed in Section 12.4, or that have long rise and fall times. Such signals typically occur in physically long connections, such as input-output buses and computer interface cables. Noise immunity is important in these applications because long signal lines are more likely to have reflections or to pick up noise from adjacent signal lines, circuits, and appliances.

Copyright © 1999 by John F. Wakerly Copying Prohibited



(b)

EN	A	B	C	D	*Q1*	*Q2*	OUT
L	L	H	H	L	off	off	Hi-Z
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H

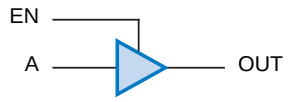


Figure 3-48 CMOS three-state buffer: (a) circuit diagram; (b) function table; (c) logic symbol.

3.7.3 Three-State Outputs

high impedance state
Hi-Z state
floating state

Logic outputs have two normal states, LOW and HIGH, corresponding to logic values 0 and 1. However, some outputs have a third electrical state that is not a logic state at all, called the *high impedance*, *Hi-Z*, or *floating state.* In this state, the output behaves as if it isn't even connected to the circuit, except for a small leakage current that may flow into or out of the output pin. Thus, an output can have one of three states—logic 0, logic 1, and Hi-Z.

three-state output
tri-state output

An output with three possible states is called (surprise!) a *three-state output* or, sometimes, a *tri-state output*. Three-state devices have an extra input, usually called "output enable" or "output disable," for placing the device's output(s) in the high-impedance state.

three-state bus

A *three-state bus* is created by wiring several three-state outputs together. Control circuitry for the "output enables" must ensure that at most one output is enabled (not in its Hi-Z state) at any time. The single enabled device can transmit logic levels (HIGH and LOW) on the bus. Examples of three-state bus design are given in Section 5.6.

three-state buffer

A circuit diagram for a CMOS *three-state buffer* is shown in Figure 3-48(a). To simplify the diagram, the internal NAND, NOR, and inverter functions are shown in functional rather than transistor form; they actually use a total of 10 transistors (see Exercise 3.79). As shown in the function table (b), when the enable (EN) input is LOW, both output transistors are off, and the output is in the Hi-Z state. Otherwise, the output is HIGH or LOW as controlled by

LEGAL NOTICE "TRI-STATE" is a trademark of National Semiconductor Corporation. Their lawyer thought you'd like to know.

Copyright © 1999 by John F. Wakerly Copying Prohibited

the "data" input A. Logic symbols for three-state buffers and gates are normally drawn with the enable input coming into the top, as shown in (c).

In practice, the three-state control circuit may be different from what we have shown, in order to provide proper dynamic behavior of the output transistors during transitions to and from the Hi-Z state. In particular, devices with three-state outputs are normally designed so that the output-enable delay (Hi-Z to LOW or HIGH) is somewhat longer than the output-disable delay (LOW or HIGH to Hi-Z). Thus, if a control circuit activates one device's output-enable input at the same time that it deactivates a second's, the second device is guaranteed to enter the Hi-Z state before the first places a HIGH or LOW level on the bus.

If two three-state outputs on the same bus are enabled at the same time and try to maintain opposite states, the situation is similar to tying standard active-pull-up outputs together as in Figure 3-56 on page 129—a nonlogic voltage is produced on the bus. If fighting is only momentary, the devices probably will not be damaged, but the large current drain through the tied outputs can produce noise pulses that affect circuit behavior elsewhere in the system.

There is a leakage current of up to 10 μA associated with a CMOS three-state output in its Hi-Z state. This current, as well as the input currents of receiving gates, must be taken into account when calculating the maximum number of devices that can be placed on a three-state bus. That is, in the LOW or HIGH state, an enabled three-state output must be capable of sinking or sourcing up to 10 μA of leakage current for every other three-state output on the bus, as well as handling the current required by every input on the bus. As with standard CMOS logic, separate LOW-state and HIGH-state calculations must be made to ensure that the fanout requirements of a particular circuit configuration are met.

*3.7.4 Open-Drain Outputs

The *p*-channel transistors in CMOS output structures are said to provide *active pull-up*, since they actively pull up the output voltage on a LOW-to-HIGH transition. These transistors are omitted in gates with *open-drain outputs*, such as the NAND gate in Figure 3-49(a). The drain of the topmost *n*-channel transistor is left unconnected internally, so if the output is not LOW it is "open," as indicated in (b). The underscored diamond in the symbol in (c) is sometimes used to indicate an open-drain output. A similar structure, called an "open-collector output," is provided in TTL logic families as described in Section 3.10.5.

active pull-up
open-drain output

An open-drain output requires an external *pull-up resistor* to provide *passive pull-up* to the HIGH level. For example, Figure 3-50 shows an open-drain CMOS NAND gate, with its pull-up resistor, driving a load.

pull-up resistor
passive pull-up

For the highest possible speed, an open-drain output's pull-up resistor should be as small as possible; this minimizes the *RC* time constant for LOW-to-

* Throughout this book, optional sections are marked with an asterisk.

Copyright © 1999 by John F. Wakerly Copying Prohibited

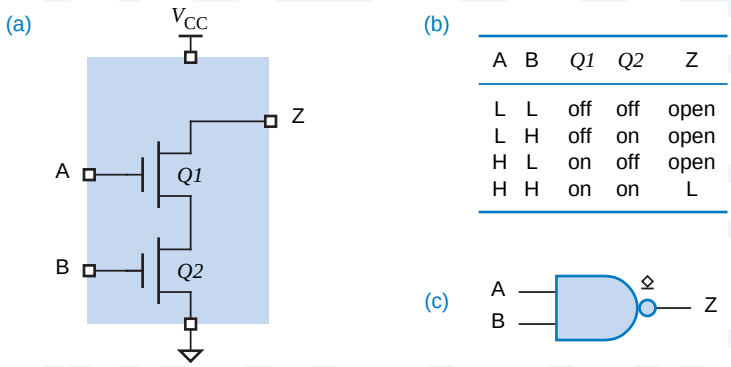


Figure 3-49
Open-drain CMOS NAND gate: (a) circuit diagram; (b) function table; (c) logic symbol.

HIGH transitions (rise time). However, the pull-up resistance cannot be arbitrarily small; the minimum resistance is determined by the open-drain output's maximum sink current, I_{OLmax}. For example, in HC- and HCT-series CMOS, I_{OLmax} is 4 mA, and the pull-up resistor can be no less than 5.0 V/4 mA, or 1.25 kΩ. Since this is an order of magnitude greater than the "on" resistance of the *p*-channel transistors in a standard CMOS gate, the LOW-to-HIGH output transitions are much slower for an open-drain gate than for standard gate with active pull-up.

As an example, let us assume that the open-drain gate in Figure 3-50 is HC-series CMOS, the pull-up resistance is 1.5 kΩ, and the load capacitance is 100 pF. We showed in Section 3.5.2 that the "on" resistance of an HC-series CMOS output in the LOW state is about 80 Ω. Thus, the *RC* time constant for a HIGH-to-LOW transition is about 80 Ω · 100 pF = 8 ns, and the output's fall time is about 8 ns. However, the *RC* time constant for a LOW-to-HIGH transition is about 1.5 kΩ · 100 pF = 150 ns, and the rise time is about 150 ns. This relatively slow rise time is contrasted with the much faster fall time in Figure 3-51. A friend of the author calls such slow rising transitions *ooze*.

ooze

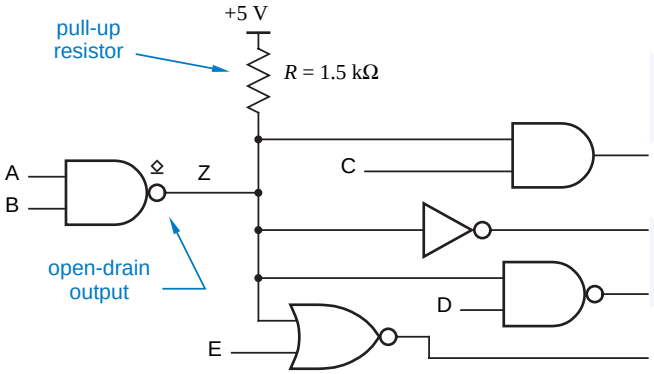


Figure 3-50
Open-drain CMOS NAND gate driving a load.

Copyright © 1999 by John F. Wakerly Copying Prohibited

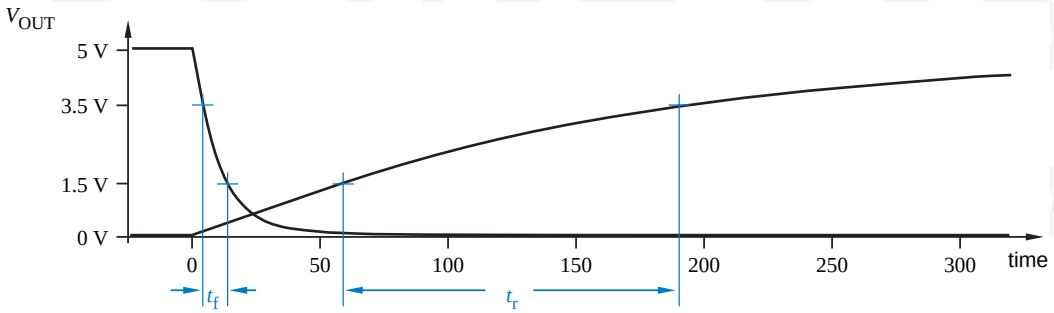


Figure 3-51 Rising and falling transitions of an open-drain CMOS output.

So why use open-drain outputs? Despite slow rise times, they can be useful in at least three applications: driving light-emitting diodes (LEDs) and other devices; performing wired logic; and driving multisource buses.

*3.7.5 Driving LEDs

An open-drain output can drive an LED as shown in Figure 3-52. If either input A or B is LOW, the corresponding *n*-channel transistor is off and the LED is off. When A and B are both HIGH, both transistors are on, the output Z is LOW, and the LED is on. The value of the pull-up resistor *R* is chosen so that the proper amount of current flows through the LED in the "on" state.

Typical LEDs require 10 mA for normal brightness. HC- and HCT-series CMOS outputs are only specified to sink or source 4 mA and are not normally used to drive LEDs. However, the outputs in advanced CMOS families such as 74AC and 74ACT can sink 24 mA or more, and can be used quite effectively to drive LEDs.

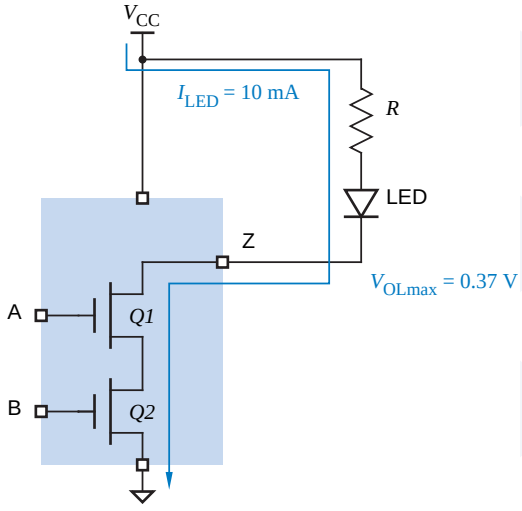


Figure 3-52
Driving an LED with an open-drain output.

Copyright © 1999 by John F. Wakerly Copying Prohibited

Three pieces of information are needed to calculate the proper value of the pull-up resistor R:

1. The LED current I_{LED} needed for the desired brightness, 10 mA for typical LEDs.
2. The voltage drop V_{LED} across the LED in the "on" condition, about 1.6 V for typical LEDs.
3. The output voltage V_{OL} of the open-drain output that sinks the LED current. In the 74AC and 74ACT CMOS families, V_{OLmax} is 0.37 V. If an output can sink I_{LED} and maintain a lower voltage, say 0.2 V, then the calculation below yields a resistor value that is a little too low, but normally with no harm done. A little more current than I_{LED} will flow and the LED will be just a little brighter than expected.

Using the above information, we can write the following equation:

$$V_{OL} + V_{LED} + (I_{LED} \cdot R) = V_{CC}$$

Assuming $V_{CC} = 5.0$ V and the other typical values above, we can solve for the required value of R:

$$R = \frac{V_{CC} - V_{OL} - V_{LED}}{I_{LED}}$$
$$= (5.0 - 0.37 - 1.6)\ \text{V}/10\ \text{mA} = 303\ \Omega$$

Note that you don't have to use an open-drain output to drive an LED. Figure 3-53(a) shows an LED driven by ordinary an CMOS NAND-gate output with active pull-up. If both inputs are HIGH, the bottom (*n*-channel) transistors pull the output LOW as in the open-drain version. If either input is LOW, the output is HIGH; although one or both of the top (*p*-channel) transistors is on, no current flows through the LED.

With some CMOS families, you can turn an LED "on" when the output is in the HIGH state, as shown in Figure 3-53(b). This is possible if the output can source enough current to satisfy the LED's requirements. However, method (b) isn't used as often as method (a), because most CMOS and TTL outputs cannot source as much current in the HIGH state as they can sink in the LOW state.

RESISTOR VALUES

In most applications, the precise value of LED series resistors is unimportant, as long as groups of nearby LEDs have similar drivers and resistors to give equal apparent brightness. In the example in this subsection, one might use an off-the-shelf resistor value of 270, 300, or 330 ohms, whatever is readily available.

Copyright © 1999 by John F. Wakerly Copying Prohibited

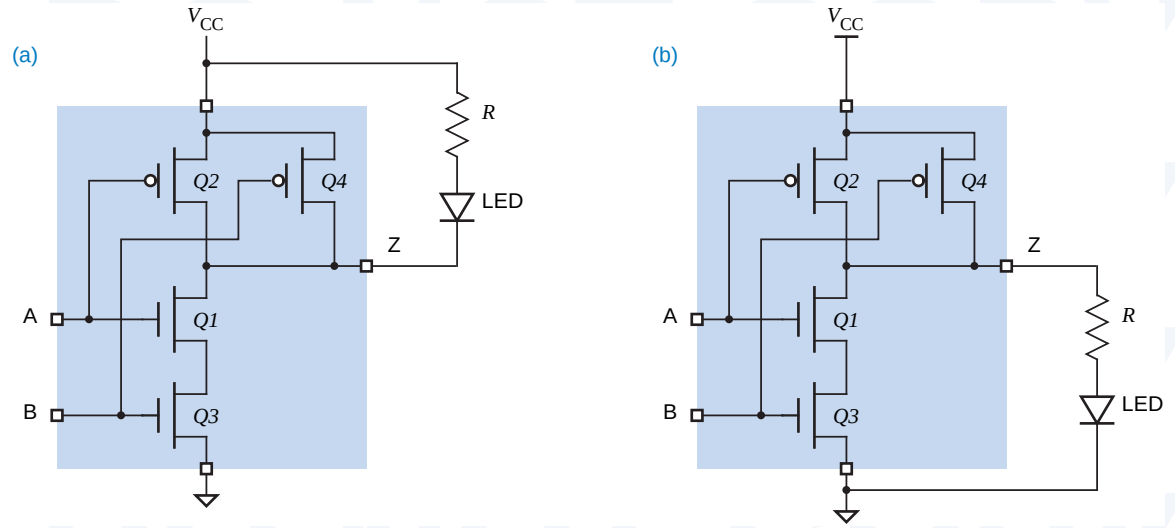


Figure 3-53 Driving an LED with an ordinary CMOS output: (a) sinking current, "on" in the LOW state; (b) sourcing current, "on" in the HIGH state.

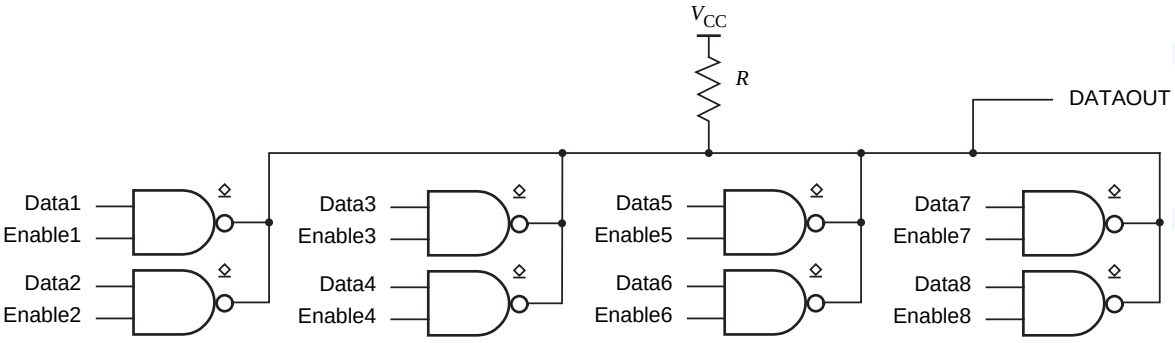
*3.7.6 Multisource Buses

open-drain bus

Open-drain outputs can be tied together to allow several devices, one at a time, to put information on a common bus. At any time all but one of the outputs on the bus are in their HIGH (open) state. The remaining output either stays in the HIGH state or pulls the bus LOW, depending on whether it wants to transmit a logical 1 or a logical 0 on the bus. Control circuitry selects the particular device that is allowed to drive the bus at any time.

For example, in Figure 3-54, eight 2-input open-drain NAND-gate outputs drive a common bus. The top input of each NAND gate is a data bit, and the

Figure 3-54 Eight open-drain outputs driving a bus.



Copyright © 1999 by John F. Wakerly Copying Prohibited

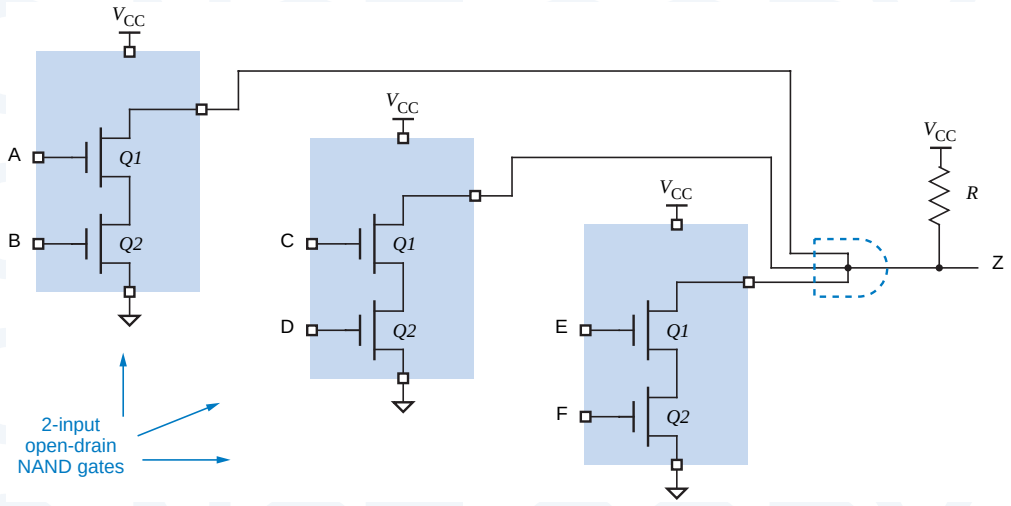


Figure 3-55 Wired-AND function on three open-drain NAND-gate outputs.

bottom input of each is a control bit. At most one control bit is HIGH at any time, enabling the corresponding data bit to be passed through to the bus. (Actually, the complement of the data bit is placed on the bus.) The other gate outputs are HIGH, that is, "open," so the data input of the enabled gate determines the value on the bus.

*3.7.7 Wired Logic

wired logic

If the outputs of several open-drain gates are tied together with a single pull-up resistor, then *wired logic* is performed. (That's *wired*, not *weird*!) An AND function is obtained, since the wired output is HIGH if and only if all of the individual gate outputs are HIGH (actually, open); any output going LOW is sufficient to pull the wired output LOW. For example, a three-input *wired AND* function is shown in Figure 3-55. If any of the individual 2-input NAND gates has both inputs HIGH, it pulls the wired output LOW; otherwise, the pull-up resistor *R* pulls the wired output HIGH.

wired AND

Note that wired logic cannot be performed using gates with active pull-up. Two such outputs wired together and trying to maintain opposite logic values result in a very high current flow and an abnormal output voltage. Figure 3-56 shows this situation, which is sometimes called *fighting*. The exact output voltage depends on the relative "strengths" of the fighting transistors, but with 5-V CMOS devices it is typically about 1–2 V, almost always a nonlogic voltage. Worse, if outputs are left fighting continuously for more than a few seconds, the chips can get hot enough to sustain internal damage *and* to burn your fingers!

fighting

Copyright © 1999 by John F. Wakerly Copying Prohibited

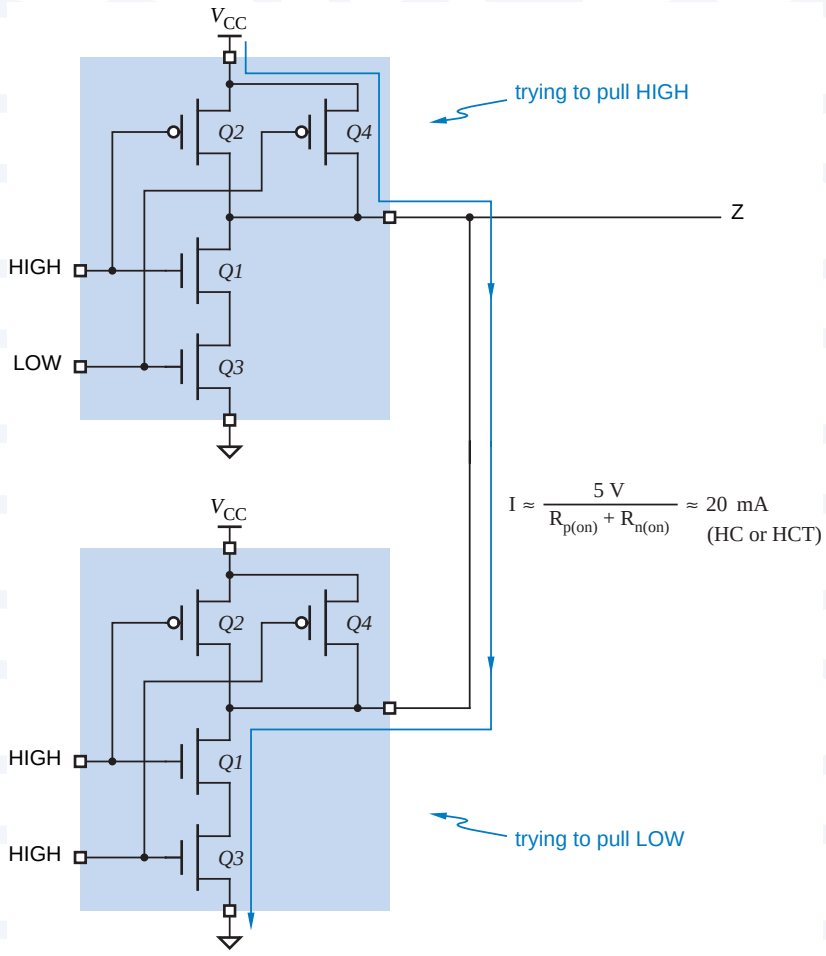


Figure 3-56
Two CMOS outputs trying to maintain opposite logic values on the same line.

*3.7.8 Pull-Up Resistors

pull-up resistor calculation

A proper choice of value for the pull-up resistor R must be made in open-drain applications. Two calculations are made to bracket the allowable values of R:

Minimum The sum of the current through R in the LOW state and the LOW-state input currents of the gates driven by the wired outputs must not exceed the LOW-state driving capability of the active output, 4 mA for HC and HCT, 24 mA for AC and ACT.

Maximum The voltage drop across R in the HIGH state must not reduce the output voltage below 2.4 V, which is V_{IHmin} for typical driven gates plus a 400-mV noise margin. This drop is produced by the HIGH-state output leakage current of the wired outputs and the HIGH-state input currents of the driven gates.

Copyright © 1999 by John F. Wakerly Copying Prohibited

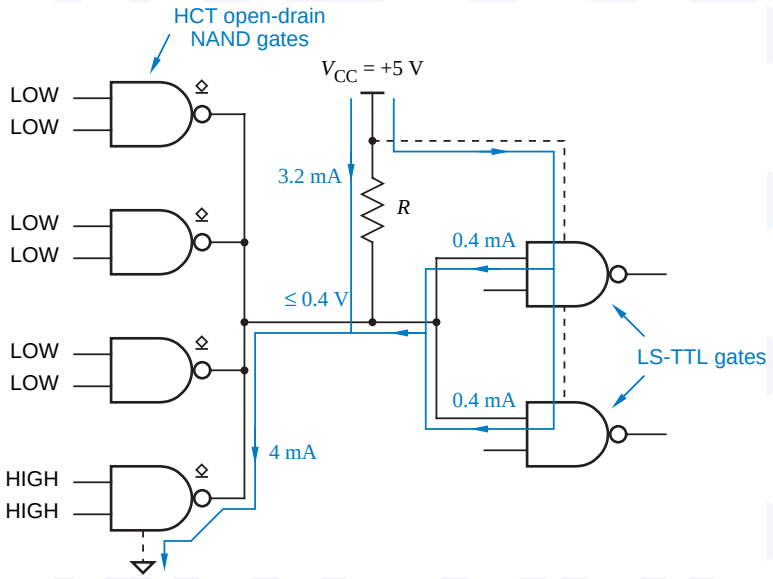


Figure 3-57
Four open-drain outputs driving two inputs in the LOW state.

For example, suppose that four HCT open-drain outputs are wired together and drive two LS-TTL inputs (Section 3.11) as shown in Figure 3-57. A LOW output must sink 0.4 mA from each LS-TTL input as well as sink the current through the pull-up resistor *R*. For the total current to stay within the HCT I_{OLmax} spec of 4 mA, the current through *R* may be no more than

$$I_{R(max)} = 4 - (2 \cdot 0.4) = 3.2 \text{ mA}$$

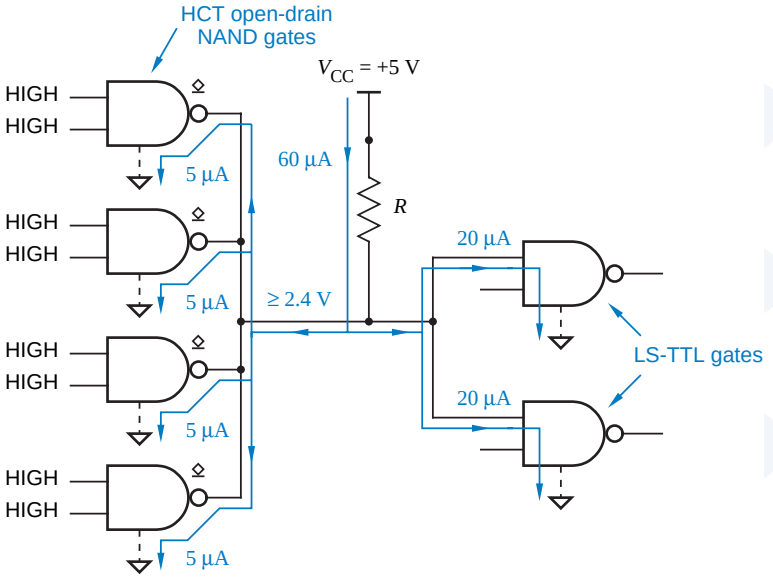


Figure 3-58
Four open-drain outputs driving two inputs in the HIGH state.

Copyright © 1999 by John F. Wakerly Copying Prohibited

Assuming that V_{OL} of the open-drain output is 0.0 V, the minimum value of R is

$$R_{min} = (5.0 - 0.0)/I_{R(max)} = 1562.5\ \Omega$$

In the HIGH state, typical open-drain outputs have a maximum leakage current of 5 μA, and typical LS-TTL inputs require 20 μA of source current. Hence, the HIGH-state current requirement as shown in Figure 3-58 is

$$I_{R(leak)} = (4 \cdot 5) + (2 \cdot 20) = 60\ \mu A$$

This current produces a voltage drop across R, and must not lower the output voltage below $V_{OHmin} = 2.4$ V; thus the maximum value of R is

$$R_{max} = (5.0 - 2.4)/I_{R(leak)} = 43.3\ \Omega$$

Hence, any value of R between 1562.5 Ω and 43.3 kΩ may be used. Higher values reduce power consumption and improve the LOW-state noise margin, while lower values increase power consumption but improve both the HIGH-state noise margin and the speed of LOW-to-HIGH output transitions.

OPEN-DRAIN ASSUMPTION

In our open-drain resistor calculations, we assume that the output voltage can be as low as 0.0 V rather than 0.4 V (V_{OLmax}) in order to obtain a worst-case result. That is, even if the open-drain output is so strong that it can pull the output voltage all the way down to 0.0 V (it's only required to pull down to 0.4 V), we'll never allow it to sink more than 4 mA, so it doesn't get overstressed. Some designers prefer to use 0.4 V in this calculation, figuring that if the output is so good that it can pull lower than 0.4 V, a little bit of excess sink current beyond 4 mA won't hurt it.

3.8 CMOS Logic Families

4000-series CMOS

The first commercially successful CMOS family was *4000-series CMOS*. Although 4000-series circuits offered the benefit of low power dissipation, they were fairly slow and were not easy to interface with the most popular logic family of the time, bipolar TTL. Thus, the 4000 series was supplanted in most applications by the more capable CMOS families discussed in this section.

All of the CMOS devices that we discuss have part numbers of the form "74FAM*nn*," where "FAM" is an alphabetic family mnemonic and *nn* is a numeric function designator. Devices in different families with the same value of *nn* perform the same function. For example, the 74HC30, 74HCT30, 74AC30, 74ACT30, and 74AHC30 are all 8-input NAND gates.

The prefix "74" is simply a number that was used by an early, popular supplier of TTL devices, Texas Instruments. The prefix "54" is used for identical parts that are specified for operation over a wider range of temperature and power-supply voltage, for use in military applications. Such parts are usually

Copyright © 1999 by John F. Wakerly Copying Prohibited

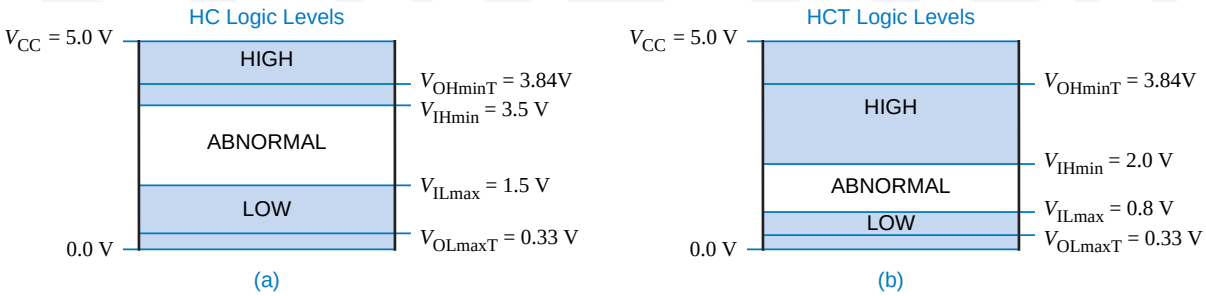


Figure 3-59 Input and output levels for CMOS devices using a 5-V supply: (a) HC; (b) HCT.

fabricated in the same way as their 74-series counterparts, except that they are tested, screened, and marked differently, a lot of extra paperwork is generated, and a higher price is charged, of course.

3.8.1 HC and HCT

HC (High-speed CMOS)

HCT (High-speed CMOS, TTL compatible)

The first two 74-series CMOS families are *HC (High-speed CMOS)* and *HCT (High-speed CMOS, TTL compatible)*. Compared with the original 4000 family, HC and HCT both have higher speed and better current sinking and sourcing capability. The HCT family uses a power supply voltage V_{CC} of 5 V and can be intermixed with TTL devices, which also use a 5-V supply.

The HC family is optimized for use in systems that use CMOS logic exclusively, and can use any power supply voltage between 2 and 6 V. A higher voltage is used for higher speed, and a lower voltage for lower power dissipation. Lowering the supply voltage is especially effective, since most CMOS power dissipation is proportional to the square of the voltage (CV^2f power).

Even when used with a 5-V supply, HC devices are not quite compatible with TTL. In particular, HC circuits are designed to recognize CMOS input levels. Assuming a supply voltage of 5.0 V, Figure 3-59(a) shows the input and output levels of HC devices. The output levels produced by TTL devices do not quite match this range, so HCT devices use the different input levels shown in (b). These levels are established in the fabrication process by making transistors with different switching thresholds, producing the different transfer characteristics shown in Figure 3-60.

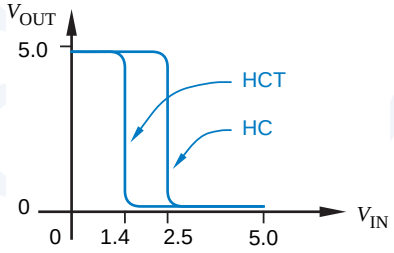


Figure 3-60
Transfer characteristics of HC and HCT circuits under typical conditions.

Copyright © 1999 by John F. Wakerly Copying Prohibited

We'll have more to say about CMOS/TTL interfacing in Section 3.12. For now, it is useful simply to note that HC and HCT are essentially identical in their output specifications; only their input levels differ.

3.8.2 VHC and VHCT

VHC (Very High-speed CMOS)

VHCT (Very High-speed CMOS, TTL compatible)

Several new CMOS families were introduced in the 1980s and the 1990s. Two of the most recent and probably the most versatile are *VHC (Very High-Speed CMOS)* and *VHCT (Very High-Speed CMOS, TTL compatible)*. These families are about twice as fast as HC/HCT while maintaining backwards compatibility with their predecessors. Like HC and HCT, the VHC and VHCT families differ from each other only in the input levels that they recognize; their output characteristics are the same.

symmetric output drive

Also like HC/HCT, VHC/VHCT outputs have *symmetric output drive*. That is, an output can sink or source equal amounts of current; the output is just as "strong" in both states. Other logic families, including the FCT and TTL families introduced later, have *asymmetric output drive;* they can sink much more current in the LOW state than they can source in the HIGH state.

asymmetric output drive

3.8.3 HC, HCT, VHC, and VHCT Electrical Characteristics

Electrical characteristics of the HC, HCT, VHC, and VHCT families are summarized in this subsection. The specifications assume that the devices are used with a nominal 5-V power supply, although (derated) operation is possible with any supply voltage in the range 2–5.5 V (up to 6 V for HC/HCT). We'll take a closer look at low-voltage and mixed-voltage operation in Section 3.13.

Commercial (74-series) parts are intended to be operated at temperatures between 0°C and 70°C, while military (54-series) parts are characterized for operation between −55°C and 125°C. The specs in Table 3-5 assume an operating temperature of 25°C. A full manufacturer's data sheet provides additional specifications for device operation over the entire temperature range.

Most devices within a given logic family have the same electrical specifications for inputs and outputs, typically differing only in power consumption and propagation delay. Table 3-5 includes specifications for a 74x00 two-input NAND gate and a 74x138 3-to-8 decoder in the HC, HCT, VHC, and VHCT families. The '00 NAND gate is included as the smallest logic-design building block in each family, while the '138 is a "medium-scale" part containing the equivalent of about 15 NAND gates. (The '138 spec is included to allow comparison with

VERY=ADVANCED, SORT OF

The VHC and VHCT logic families are manufactured by several companies, including Motorola, Fairchild, and Toshiba. Compatible families with similar but not identical specifications are manufactured by Texas Instruments and Philips; they are called AHC and AHCT, where the "A" stands for "Advanced."

Copyright © 1999 by John F. Wakerly Copying Prohibited

Table 3-5 Speed and power characteristics of CMOS families operating at 5 V

Description	Part	Symbol	Condition	Family			
				HC	HCT	VHC	VHCT
Typical propagation delay (ns)	’00	t_{PD}		9	10	5.2	5.5
	’138			18	20	7.2	8.1
Quiescent power-supply current (μA)	’00	I_{CC}	$V_{in} = 0$ or V_{CC}	2.5	2.5	5.0	5.0
	’138		$V_{in} = 0$ or V_{CC}	40	40	40	402
Quiescent power dissipation (mW)	’00		$V_{in} = 0$ or V_{CC}	0.0125	0.0125	0.025	0.025
	’138		$V_{in} = 0$ or V_{CC}	0.2	0.2	0.2	0.2
Power dissipation capacitance (pF)	’00	C_{PD}		22	15	19	17
	’138	C_{PD}		55	51	34	49
Dynamic power dissipation (mW/MHz)	’00			0.55	0.38	0.48	0.43
	’138			1.38	1.28	0.85	1.23
Total power dissipation (mW)	’00		$f = 100$ kHz	0.068	0.050	0.073	0.068
	’00		$f = 1$ MHz	0.56	0.39	0.50	0.45
	’00		$f = 10$ MHz	5.5	3.8	4.8	4.3
	’138		$f = 100$ kHz	0.338	0.328	0.285	0.323
	’138		$f = 1$ MHz	1.58	1.48	1.05	1.43
	’138		$f = 10$ MHz	14.0	13.0	8.7	12.5
Speed-power product (pJ)	’00		$f = 100$ kHz	0.61	0.50	0.38	0.37
	’00		$f = 1$ MHz	5.1	3.9	2.6	2.5
	’00		$f = 10$ MHz	50	38	25	24
	’138		$f = 100$ kHz	6.08	6.55	2.05	2.61
	’138		$f = 1$ MHz	28.4	29.5	7.56	11.5
	’138		$f = 10$ MHz	251	259	63	101

the faster FCT family in Section 3.8.4; ’00 gates are not manufactured in the FCT family.)

The first row of Table 3-5 specifies propagation delay. As discussed in Section 3.6.2, two numbers, t_{pHL} and t_{pLH} may be used to specify delay; the number in the table is the worst-case of the two. Skipping ahead to Table 3-11 on page 163, you can see that HC and HCT are about the same speed as LS TTL, and that VHC and VHCT are almost as fast as ALS TTL. The propagation delay

NOTE ON NOTATION The “x” in the notation“74x00” takes the place of a family designator such as HC, HCT, VHC, VHCT, FCT, LS, ALS, AS, or F. We may also refer to such a generic part simply as a “ ’00” and leave off the “74x.”

Copyright © 1999 by John F. Wakerly Copying Prohibited

QUIETLY GETTING MORE DISS'ED

HCT and VHCT circuits can also be driven by TTL devices, which may produce HIGH output levels as low as 2.4 V. As we explained in Section 3.5.3, a CMOS output may draw additional current from the power supply if any of the inputs are nonideal. In the case of an HCT or VHCT inverter with a HIGH input of 2.4 V, the bottom, *n*-channel output transistor is fully "on." However, the top, *p*-channel transistor is also partially "on." This allows the additional quiescent current flow, specified as ΔI_{CC} or I_{CCT} in the data sheet, which can be as much as 2–3 mA per nonideal input in HCT and VHCT devices.

for the '138 is somewhat longer than for the '00, since signals must travel through three or four levels of gates internally.

The second and third rows of the table show that the quiescent power dissipation of these CMOS devices is practically nil, well under a milliwatt (mW) if the inputs have CMOS levels—0 V for LOW and V_{CC} for HIGH. (Note that in the table, the quiescent power dissipation numbers given for the '00 are per gate, while for the '138 they apply to the entire MSI device.)

As we discussed in Section 3.6.3, the dynamic power dissipation of a CMOS gate depends on the voltage swing of the output (usually V_{CC}), the output transition frequency (f), and the capacitance that is being charged and discharged on transitions, according to the formula

$$P_D = (C_L + C_{PD}) \cdot V_{DD}^2 \cdot f$$

Here, C_{PD} is the power dissipation capacitance of the device and C_L is the capacitance of the load attached to the CMOS output in a given application. The table lists both C_{PD} and an equivalent dynamic power dissipation factor in units of milliwatts per megahertz, assuming that $C_L = 0$. Using this factor, the total power dissipation is computed at various frequencies as the sum of the dynamic power dissipation at that frequency and the quiescent power dissipation.

speed-power product

Shown next in the table, the *speed-power product* is simply the product of the propagation delay and power consumption of a typical gate; the result is measured in picojoules (pJ). Recall from physics that the joule is a unit of energy, so the speed-power product measures a sort of efficiency—how much energy a logic gate uses to switch its output. In this day and age, it's obvious that the lower the energy usage, the better.

SAVING ENERGY

There are practical as well as geopolitical reasons for saving energy in digital systems. Lower energy consumption means lower cost of power supplies and cooling systems. Also, a digital system's reliability is improved more by running it cooler than by any other single reliability improvement strategy.

Copyright © 1999 by John F. Wakerly Copying Prohibited

Table 3-6 Input specifications for CMOS families with V_{CC} between 4.5 and 5.5 V.

Description	Symbol	Condition	Family			
			HC	HCT	VHC	VHCT
Input leakage current (μA)	I_{Imax}	V_{in} = any	±1	±1	±1	±1
Maximum input capacitance (pF)	C_{INmax}		10	10	10	10
LOW-level input voltage (V)	V_{ILmax}		1.35	0.8	1.35	0.8
HIGH-level input voltage (V)	V_{IHmin}		3.85	2.0	3.85	2.0

Table 3-6 gives the input specs of typical CMOS devices in each of the families. Some of the specs assume that the 5-V supply has a ±10% margin; that is, V_{CC} can be anywhere between 4.5 and 5.5 V. These parameters were discussed in previous sections, but for reference purposes their meanings are summarized here:

I_{Imax} The maximum input current for any value of input voltage. This spec states that the current flowing into or out of a CMOS input is 1 μA or less for any value of input voltage. In other words, CMOS inputs create almost no DC load on the circuits that drive them.

C_{INmax} The maximum capacitance of an input. This number can be used when figuring the AC load on an output that drives this and other inputs. Most manufacturers also specify a lower, typical input capacitance of about 5 pF, which gives a good estimate of AC load if you're not unlucky.

V_{ILmax} The maximum voltage that an input is guaranteed to recognize as LOW. Note that the values are different for HC/VHC versus HCT/VHCT. The "CMOS" value, 1.35 V, is 30% of the minimum power-supply voltage, while the "TTL" value is 0.8 V for compatibility with TTL families.

CMOS VS. TTL POWER DISSIPATION

At high transition frequencies (f), CMOS families actually use more power than TTL. For example, compare HCT CMOS in Table 3-5 at f = 10 MHz with LS TTL in Table 3-11; a CMOS gate uses three times as much power as a TTL gate at this frequency. Both HCT and LS may be used in systems with maximum "clock" frequencies of up to about 20 MHz, so you might think that CMOS is not so good for high-speed systems. However, the transition frequencies of most outputs in typical systems are much less than the maximum frequency present in the system (e.g., see Exercise 3.76). Thus, typical CMOS systems have a lower total power dissipation than they would have if they were built with TTL.

Copyright © 1999 by John F. Wakerly Copying Prohibited

Table 3-7 Output specifications for CMOS families operating with V_{CC} between 4.5 and 5.5 V.

Description	Symbol	Condition	Family HC	HCT	VHC	VHCT
LOW-level output current (mA)	I_{OLmaxC}	CMOS load	0.02	0.02	0.05	0.05
	I_{OLmaxT}	TTL load	4.0	4.0	8.0	8.0
LOW-level output voltage (V)	V_{OLmaxC}	$I_{out} \le I_{OLmaxC}$	0.1	0.1	0.1	0.1
	V_{OLmaxT}	$I_{out} \le I_{OLmaxT}$	0.33	0.33	0.44	0.44
HIGH-level output current (mA)	I_{OHmaxC}	CMOS load	–0.02	–0.02	–0.05	–0.05
	I_{OHmaxT}	TTL load	–4.0	–4.0	–8.0	–8.0
HIGH-level output voltage (V)	V_{OHminC}	$\|I_{out}\| \le \|I_{OHmaxC}\|$	4.4	4.4	4.4	4.4
	V_{OHminT}	$\|I_{out}\| \le \|I_{OHmaxT}\|$	3.84	3.84	3.80	3.80

V_{IHmin} The minimum voltage that an input is guaranteed to recognize as HIGH. The "CMOS" value, 3.85 V, is 70% of the maximum power-supply voltage, while the "TTL" value is 2.0 V for compatibility with TTL families. (Unlike CMOS levels, TTL input levels are not symmetric with respect to the power-supply rails.)

The specifications for TTL-compatible CMOS outputs usually have two sets of output parameters; one set or the other is used depending on how an output is loaded. A *CMOS load* is one that requires the output to sink and source very little DC current, 20 μA for HC/HCT and 50 μA for VHC/VHCT. This is, of course, the case when the CMOS outputs drive only CMOS inputs. With CMOS loads, CMOS outputs maintain an output voltage within 0.1 V of the supply rails, 0 and V_{CC}. (A worst-case V_{CC} = 4.5 V is used for the table entries; hence, V_{OHminC} = 4.4 V.)

CMOS load

A *TTL load* can consume much more sink and source current, up to 4 mA from and HC/HCT output and 8 mA from a VHC/VHCT output. In this case, a higher voltage drop occurs across the "on" transistors in the output circuit, but the output voltage is still guaranteed to be within the normal range of TTL output levels.

TTL load

Table 3-7 lists CMOS output specifications for both CMOS and TTL loads. These parameters have the following meanings:

I_{OLmaxC} The maximum current that an output can supply in the LOW state while driving a CMOS load. Since this is a positive value, current flows *into* the output pin.

I_{OLmaxT} The maximum current that an output can supply in the LOW state while driving a TTL load.

Copyright © 1999 by John F. Wakerly Copying Prohibited

V_{OLmaxC} The maximum voltage that a LOW output is guaranteed to produce while driving a CMOS load, that is, as long as I_{OLmaxC} is not exceeded.

V_{OLmaxT} The maximum voltage that a LOW output is guaranteed to produce while driving a TTL load, that is, as long as I_{OLmaxT} is not exceeded.

I_{OHmaxC} The maximum current that an output can supply in the HIGH state while driving a CMOS load. Since this is a negative value, positive current flows out of the output pin.

I_{OHmaxT} The maximum current that an output can supply in the HIGH state while driving a TTL load.

V_{OHminC} The minimum voltage that a HIGH output is guaranteed to produce while driving a CMOS load, that is, as long as I_{OHmaxC} is not exceeded.

V_{OHminT} The minimum voltage that a HIGH output is guaranteed to produce while driving a TTL load, that is, as long as I_{OHmaxT} is not exceeded.

The voltage parameters above determine DC noise margins. The LOW-state DC noise margin is the difference between V_{OLmax} and V_{ILmax}. This depends on the characteristics of both the driving output and the driven inputs. For example, the LOW-state DC noise margin of a HCT driving a few HCT inputs (a CMOS load) is $0.8 - 0.1 = 0.7$ V. With a TTL load, the noise margin for the HCT inputs drops to $0.8 - 0.33 = 0.47$ V. Similarly, the HIGH-state DC noise margin is the difference between V_{OHmin} and V_{IHmin}. In general, when different families are interconnected, you have to compare the appropriate V_{OLmax} and V_{OHmin} of the driving gate with V_{ILmax} and V_{IHmin} of all the driven gates to determine the worst-case noise margins.

The I_{OLmax} and I_{OHmax} parameters in the table determine fanout capability, and are especially important when an output drives inputs in one or more different families. Two calculations must be performed to determine whether an output is operating within its rated fanout capability:

HIGH-state fanout The I_{IHmax} values for all of the driven inputs are added. The sum must be less than I_{OHmax} of the driving output.

LOW-state fanout The I_{ILmax} values for all of the driven inputs are added. The sum must be less than I_{OLmax} of the driving output

Note that the input and output characteristics of specific components may vary from the representative values given in Table 3-7, so you must always consult the manufacturers' data sheets when analyzing a real design.

*3.8.4 FCT and FCT-T

FCT (Fast CMOS, TTL compatible)

In the early 1990s, yet another CMOS family was launched. The key benefit of the *FCT (Fast CMOS, TTL compatible*) family was its ability to meet or exceed the speed and the output drive capability of the best TTL families while reducing power consumption and maintaining full compatibility with TTL.

Copyright © 1999 by John F. Wakerly Copying Prohibited

The original FCT family had the drawback of producing a full 5-V CMOS V_{OH}, creating enormous CV^2f power dissipation and circuit noise as its outputs swung from 0 V to almost 5 V in high-speed (25 MHz+) applications. A variation of the family, *FCT-T (Fast CMOS, TTL compatible with TTL V_{OH})*, was quickly introduced with circuit innovations to reduce the HIGH-level output voltage, thereby reducing both power consumption and switching noise while maintaining the same high operating speed as the original FCT. A suffix of "T" is used on part numbers to denote the FCT-T output structure, for example, 74FCT138T versus 74FCT138.

FCT-T (Fast CMOS, TTL compatible with TTL V_{OH}

The FCT-T family remains very popular today. A key application of FCT-T is driving buses and other heavy loads. Compared with other CMOS families, it can source or sink gobs of current, up to 64 mA in the LOW state.

*3.8.5 FCT-T Electrical Characteristics

Electrical characteristics of the 5-V FCT-T family are summarized in Table 3-8. The family is specifically designed to be intermixed with TTL devices, so its operation is only specified with a nominal 5-V supply and TTL logic levels. Some manufacturers are beginning to sell parts with similar capabilities using a 3.3-V supply, and using the FCT designation. However, they are different devices with different part numbers.

Individual logic gates are not manufactured in the FCT family. Perhaps the simplest FCT logic element is a 74FCT138T decoder, which has six inputs, eight outputs, and contains the equivalent of about a dozen 4-input gates internally. (This function is described later, in Section 5.4.4.) Comparing its propagation delay and power consumption in Table 3-8 with the corresponding HCT and VHCT numbers in Table 3-5 on page 134, you can see that the FCT-T family is superior in both speed and power dissipation. When comparing, note that FCT-T manufacturers specify only maximum, not typical propagation delays.

Unlike other CMOS families, FCT-T does not have a C_{PD} specification. Instead, it has an I_{CCD} specification:

I_{CCD} Dynamic power supply current, in units of mA/MHz. This is the amount of additional power supply current that flows when one input is changing at the rate of 1 MHz.

EXTREME SWITCHING

Device outputs in the FCT and FCT-T families have very low impedance and as a consequence extremely fast rise and fall times. In fact, they are so fast that they are often a major source of "analog" problems, including switching noise and "ground bounce," so extra care must be taken in the analog and physical design of printed-circuit boards using these and other extremely high-speed parts. To reduce the effects of transmission-line reflections (Section 12.4.3), another high-speed design worry, some FCT-T outputs have built-in 25-Ω series resistors.

Copyright © 1999 by John F. Wakerly Copying Prohibited

Table 3-8 Specifications for a 74FCT138T decoder in the FCT-T logic family.

Description	*Symbol*	*Condition*	*Value*
Maximum propagation delay (ns)	t_{PD}		5.8
Quiescent power-supply current (μA)	I_{CC}	$V_{in} = 0$ or V_{CC}	200
Quiescent power dissipation (mW)		$V_{in} = 0$ or V_{CC}	1.0
Dynamic power supply current (mA/MHz)	I_{CCD}	Outputs open, one input changing	0.12
Quiescent power supply current per TTL input (mA)	ΔI_{CC}	$V_{in} = 3.4$ V	2.0
Total power dissipation (mW)		$f = 100$ kHz	0.60
		$f = 1$ MHz	1.06
		$f = 10$ MHz	1.6
Speed-power product (pJ)		$f = 100$ kHz	6.15
		$f = 1$ MHz	9.3
		$f = 10$ MHz	41
Input leakage current (μA)	I_{Imax}	V_{in} = any	±5
Typical input capacitance (pF)	C_{INtyp}		5
LOW-level input voltage (V)	V_{ILmax}		0.8
HIGH-level input voltage (V)	V_{IHmin}		2.0
LOW-level output current (mA)	I_{OLmax}		64
LOW-level output voltage (V)	V_{OLmax}	$I_{out} \le I_{OLmax}$	0.55
HIGH-level output current (mA)	I_{OHmax}		−15
HIGH-level output voltage (V)	V_{OHmin}	$\lvert I_{out}\rvert \le \lvert I_{OHmax}\rvert$	2.4
	V_{OHtyp}	$\lvert I_{out}\rvert \le \lvert I_{OHmax}\rvert$	3.3

The I_{CCD} specification gives the same information as C_{PD}, but in a different way. The circuit's internal power dissipation due to transitions at a given frequency f can be calculated by the formula

$$P_T = V_{CC} \cdot I_{CCD} \cdot f$$

Thus, I_{CCD}/V_{CC} is algebraically equivalent to the C_{PD} specification of other CMOS families (see Exercise 3.83). FCT-T also has a ΔI_{CC} specification for the extra quiescent current that is consumed with nonideal HIGH inputs (see box at the top of page 135).

Copyright © 1999 by John F. Wakerly Copying Prohibited

3.9 Bipolar Logic

Bipolar logic families use semiconductor diodes and bipolar junction transistors as the basic building blocks of logic circuits. The simplest bipolar logic elements use diodes and resistors to perform logic operations; this is called diode logic. Most TTL logic gates use diode logic internally and boost their output drive capability using transistor circuits. Some TTL gates use parallel configurations of transistors to perform logic functions. ECL gates, described in Section 3.14, use transistors as current switches to achieve very high speed.

diode logic

This section covers the basic operation of bipolar logic circuits made from diodes and transistors, and the next section covers TTL circuits in detail. Although TTL is the most commonly used bipolar logic family, it has been largely supplanted by the CMOS families that we studied in previous sections.

Still, it is useful to study basic TTL operation for the occasional application that requires TTL/CMOS interfacing, discussed in Section 3.12. Also, an understanding of TTL may give you insight into the fortuitous similarity of logic levels that allowed the industry to migrate smoothly from TTL to 5-V CMOS logic, and now to lower-voltage, higher-performance 3.3-V CMOS logic, as described in Section 3.13. If you're not interested in all the gory details of TTL, you can skip to Section 3.11 for an overview of TTL families.

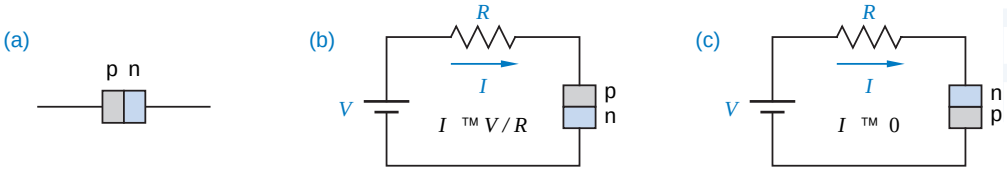
3.9.1 Diodes

A *semiconductor diode* is fabricated from two types of semiconductor material, called *p*-type and *n*-type, that are brought into contact with each other as shown in Figure 3-61(a). This is basically the same material that is used in *p*-channel and *n*-channel MOS transistors. The point of contact between the *p* and *n* materials is called a *pn junction*. (Actually, a diode is normally fabricated from a single monolithic crystal of semiconductor material in which the two halves are "doped" with different impurities to give them *p*-type and *n*-type properties.)

semiconductor diode
p-type material
n-type material
pn junction

The physical properties of a *pn* junction are such that positive current can easily flow from the *p*-type material to the *n*-type. Thus, if we build the circuit shown in Figure 3-61(b), the *pn* junction acts almost like a short circuit. However, the physical properties also make it very difficult for positive current to

Figure 3-61 Semiconductor diodes: (a) the *pn* junction; (b) forward-biased junction allowing current flow; (c) reverse-biased junction blocking current flow.



Copyright © 1999 by John F. Wakerly Copying Prohibited

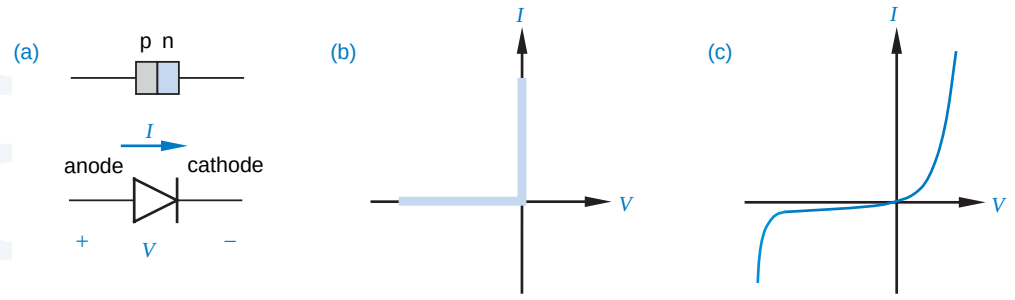


Figure 3-62 Diodes: (a) symbol; (b) transfer characteristic of an ideal diode; (c) transfer characteristic of a real diode.

flow in the opposite direction, from *n* to *p*. Thus, in the circuit of Figure 3-61(c), the *pn* junction behaves almost like an open circuit. This is called *diode action*.

diode action

Although it's possible to build vacuum tubes and other devices that exhibit diode action, modern systems use *pn* junctions—semiconductor diodes—which we'll henceforth call simply *diodes*. Figure 3-62(a) shows the schematic symbol for a diode. As we've shown, in normal operation significant amounts of current can flow only in the direction indicated by the two arrows, from *anode* to *cathode*. In effect, the diode acts like a short circuit as long as the voltage across the anode-to-cathode junction is nonnegative. If the anode-to-cathode voltage is negative, the diode acts like an open circuit and no current flows.

diode

anode
cathode

The transfer characteristic of an ideal diode shown in Figure 3-62(b) further illustrates this principle. If the anode-to-cathode voltage, *V*, is negative, the diode is said to be *reverse biased* and the current *I* through the diode is zero. If *V* is nonnegative, the diode is said to be *forward biased* and *I* can be an arbitrarily large positive value. In fact, *V* can never get larger than zero, because an ideal diode acts like a zero-resistance short circuit when forward biased.

reverse-biased diode
forward-biased diode

A nonideal, real diode has a resistance that is less than infinity when reverse biased, and greater than zero when forward biased, so the transfer characteristic looks like Figure 3-62(c). When forward biased, the diode acts like a

YES, THERE ARE TWO ARROWS

. . . in Figure 3-62(a). The second arrow is built into the diode symbol to help you remember the direction of current flow. Once you know this, there are many ways to remember which end is called the anode and which is the cathode. Aficionados of vacuum-tube hi-fi amplifiers may remember that electrons travel from the hot cathode to the anode, and therefore positive current flow is from anode to cathode. Those of us who were still watching "Sesame Street" when most vacuum tubes went out of style might like to think in terms of the alphabet—current flows alphabetically from A to C.

Copyright © 1999 by John F. Wakerly Copying Prohibited

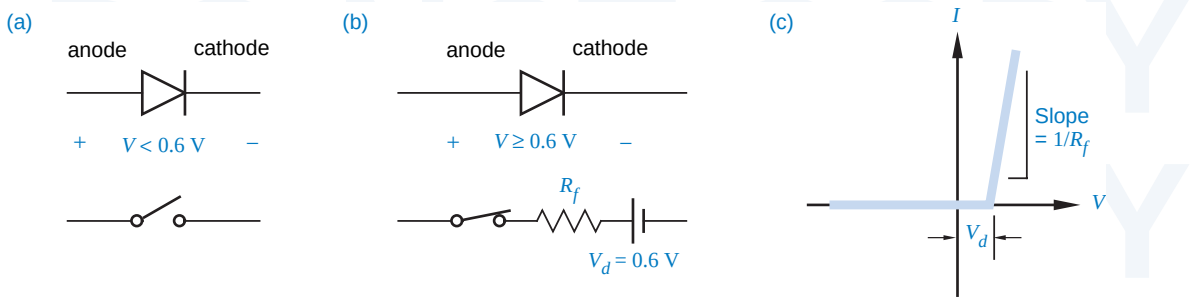


Figure 3-63 Model of a real diode: (a) reverse biased; (b) forward biased; (c) transfer characteristic of forward-biased diode.

small nonlinear resistance; its voltage drop increases as current increases, but not strictly proportionally. When the diode is reverse biased, a small amount of negative *leakage current* flows. If the voltage is made too negative, the diode *breaks down,* and large amounts of negative current can flow; in most applications, this type of operation is avoided.

leakage current
diode breakdown

A real diode can be modeled very simply as shown in Figure 3-63(a) and (b). When the diode is reverse biased, it acts like an open circuit; we ignore leakage current. When the diode is forward biased, it acts like a small resistance, R_f, in series with V_d, a small voltage source. R_f is called the *forward resistance* of the diode, and V_d is called a *diode-drop.*

forward resistance
diode-drop

Careful choice of values for R_f and V_d yields a reasonable piecewise-linear approximation to the real diode transfer characteristic, as in Figure 3-63(c). In a typical small-signal diode such as a 1N914, the forward resistance R_f is about 25 Ω and the diode-drop V_d is about 0.6 V.

In order to get a feel for diodes, you should remember that a real diode does not actually contain the 0.6-V source that appears in the model. It's just that, due to the nonlinearity of the real diode's transfer characteristic, significant amounts of current do not begin to flow until the diode's forward voltage V has reached about 0.6 V. Also note that in typical applications, the 25-Ω forward resistance of the diode is small compared to other resistances in the circuit, so that very little additional voltage drop occurs across the forward-biased diode once V has reached 0.6 V. Thus, for practical purposes, a forward-biased diode may be considered to have a fixed drop of 0.6 V or so .

ZENER DIODES *Zener diodes* take advantage of diode breakdown, in particular the steepness of the *V–I* slope in the breakdown region. A Zener diode can function as a voltage regulator when used with a resistor to limit the breakdown current. A wide variety of Zeners with different breakdown voltages are produced for voltage-regulator applications.

Copyright © 1999 by John F. Wakerly Copying Prohibited

Table 3-9
Logic levels in a simple diode logic system.

Signal Level	*Designation*	*Binary Logic Value*
0–2 volts	LOW	0
2–3 volts	noise margin	undefined
3–5 volts	HIGH	1

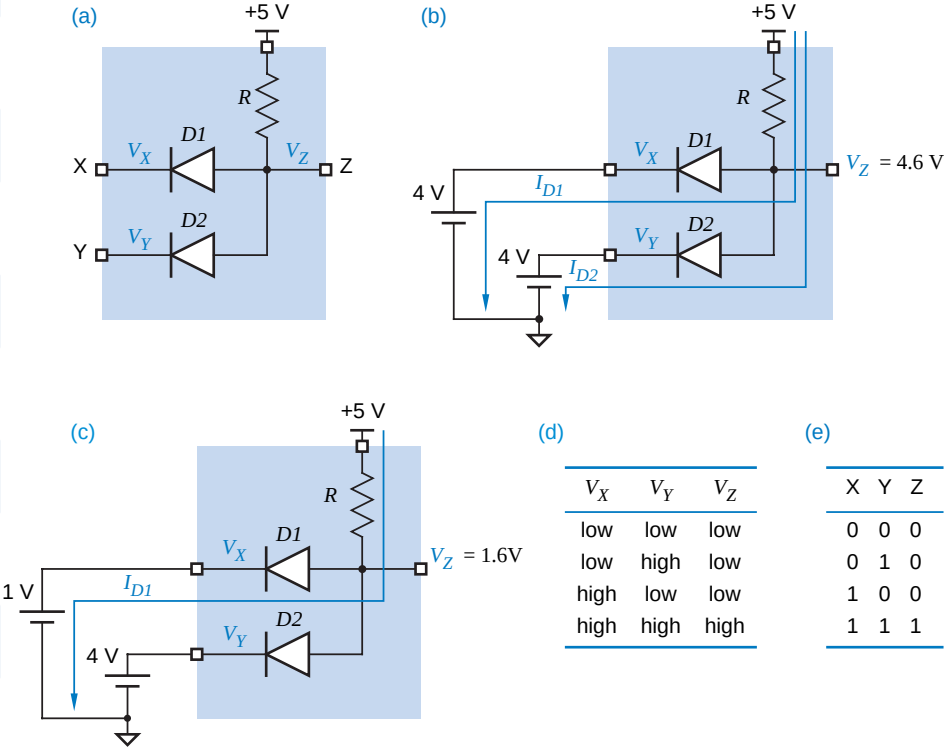
3.9.2 Diode Logic

LOW
HIGH

Diode action can be exploited to perform logical operations. Consider a logic system with a 5-V power supply and the characteristics shown in Table 3-9. Within the 5-volt range, signal voltages are partitioned into two ranges, LOW and HIGH, with a 1-volt noise margin between. A voltage in the LOW range is considered to be a logic 0, and a voltage in the HIGH range is a logic 1.

diode AND gate

With these definitions, a *diode AND gate* can be constructed as shown in Figure 3-64(a). In this circuit, suppose that both inputs X and Y are connected to HIGH voltage sources, say 4 V, so that *VX* and *VY* are both 4 V as in (b). Then both diodes are forward biased, and the output voltage *VZ* is one diode-drop above 4 V, or about 4.6 V. A small amount of current, determined by the value of *R*, flows from the 5-V supply through the two diodes and into the 4-V sources. The colored arrows in the figure show the path of this current flow.



(d)

V_X	V_Y	V_Z
low	low	low
low	high	low
high	low	low
high	high	high

(e)

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

Figure 3-64
Diode AND gate: (a) electrical circuit; (b) both inputs HIGH; (c) one input HIGH, one LOW; (d) function table; (e) truth table.

Copyright © 1999 by John F. Wakerly Copying Prohibited

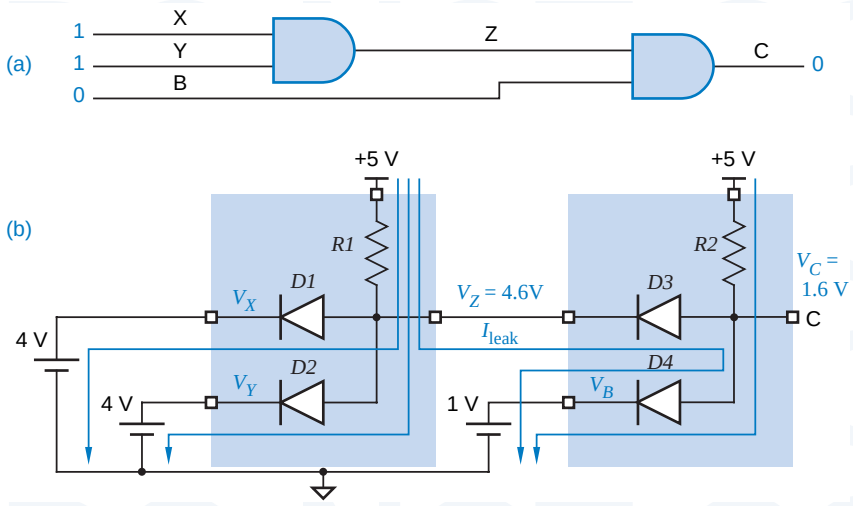


Figure 3-65
Two AND gates:
(a) logic diagram;
(b) electrical circuit.

Now suppose that *VX* drops to 1 V as in Figure 3-64(c). In the diode AND gate, the output voltage equals the lower of the two input voltages plus a diode-drop. Thus, *VZ* drops to 1.6 V, and diode *D2* is reverse biased (the anode is at 1.6 V and the cathode is still at 4 V). The single LOW input "pulls down" the output of the diode AND gate to a LOW value. Obviously, two LOW inputs create a LOW output as well. This functional operation is summarized in (d) and is repeated in terms of binary logic values in (e); clearly, this is an AND gate.

Figure 3-65(a) shows a logic circuit with two AND gates connected together; Figure 3-65(b) shows the equivalent electrical circuit with a particular set of input values. This example shows the necessity of diodes in the AND circuit: *D3* allows the output Z of the first AND gate to remain HIGH while the output C of the second AND gate is being pulled LOW by input B through *D4*.

When diode logic gates are cascaded as in Figure 3-65, the voltage levels of the logic signals move away from the power-supply rails and towards the undefined region. Thus, in practice, a diode AND gate normally must be followed by a transistor amplifier to restore the logic levels; this is the scheme used in TTL NAND gates, described in Section 3.10.1. However, logic designers are occasionally tempted to use discrete diodes to perform logic under special circumstances; for example, see Exercise 3.94.

3.9.3 Bipolar Junction Transistors

A *bipolar junction transistor* is a three-terminal device that, in most logic circuits, acts like a current-controlled switch. If we put a small current into one of the terminals, called the *base*, then the switch is "on"—current may flow between the other two terminals, called the *emitter* and the *collector*. If no current is put into the base, then the switch is "off"—no current flows between the emitter and the collector.

bipolar junction transistor
base
emitter
collector

Copyright © 1999 by John F. Wakerly Copying Prohibited

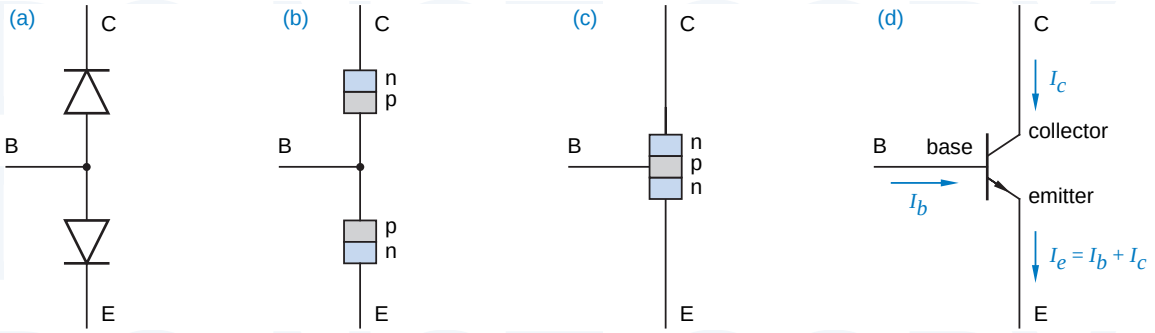


Figure 3-66 Development of an *npn* transistor: (a) back-to-back diodes; (b) equivalent *pn* junctions; (c) structure of an *npn* transistor; (d) *npn* transistor symbol.

To study the operation of a transistor, we first consider the operation of a pair of diodes connected as shown in Figure 3-66(a). In this circuit, current can flow from node B to node C or node E, when the appropriate diode is forward biased. However, no current can flow from C to E, or vice versa, since for any choice of voltages on nodes B, C, and E, one or both diodes will be reverse biased. The *pn* junctions of the two diodes in this circuit are shown in (b).

npn transistor

Now suppose that we fabricate the back-to-back diodes so that they share a common *p*-type region, as shown in Figure 3-66(c). The resulting structure is called an *npn transistor* and has an amazing property. (At least, the physicists working on transistors back in the 1950s thought it was amazing!) If we put current across the base-to-emitter *pn* junction, then current is also enabled to flow across the collector-to-base *np* junction (which is normally impossible) and from there to the emitter.

The circuit symbol for the *npn* transistor is shown in Figure 3-66(d). Notice that the symbol contains a subtle arrow in the direction of positive current flow. This also reminds us that the base-to-emitter junction is a *pn* junction, the same as a diode whose symbol has an arrow pointing in the same direction.

pnp transistor

It is also possible to fabricate a *pnp transistor*, as shown in Figure 3-67. However, *pnp* transistors are seldom used in digital circuits, so we won't discuss them any further.

amplifier
active region

The current I_e flowing out of the emitter of an *npn* transistor is the sum of the currents I_b and I_c flowing into the base and the collector. A transistor is often used as a signal *amplifier*, because over a certain operating range (the *active region*) the collector current is equal to a fixed constant times the base current ($I_c = \beta \cdot I_b$). However, in digital circuits, we normally use a transistor as a simple switch that's always fully "on" or fully "off," as explained next.

common-emitter configuration

Figure 3-68 shows the *common-emitter configuration* of an *npn* transistor, which is most often used in digital switching applications. This configuration

Copyright © 1999 by John F. Wakerly Copying Prohibited

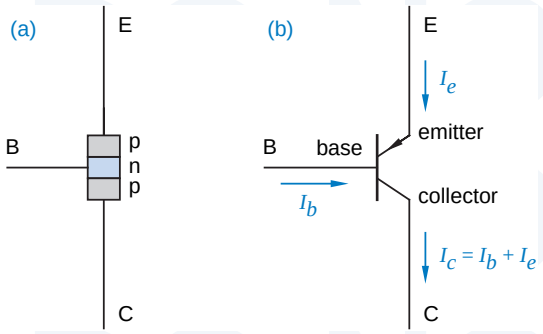


Figure 3-67
A *pnp* transistor: (a) structure; (b) symbol.

uses two discrete resistors, *R1* and *R2*, in addition to a single *npn* transistor. In this circuit, if V_{IN} is 0 or negative, then the base-to-emitter diode junction is reverse biased, and no base current (I_b) can flow. If no base current flows, then no collector current (I_c) can flow, and the transistor is said to be *cut off (OFF)*.

cut off (OFF)

Since the base-to-emitter junction is a *real* diode, as opposed to an ideal one, V_{IN} must reach at least +0.6 V (one diode-drop) before any base current can flow. Once this happens, Ohm's law tells us that

$$I_b = (V_{IN} - 0.6) / R1$$

(We ignore the forward resistance R_f of the forward-biased base-to-emitter junction, which is usually small compared to the base resistor *R1*.) When base current flows, then collector current can flow in an amount proportional to I_b, that is,

$$I_c = \beta \cdot I_b$$

The constant of proportionality, β, is called the *gain* of the transistor, and is in the range of 10 to 100 for typical transistors.

β
gain

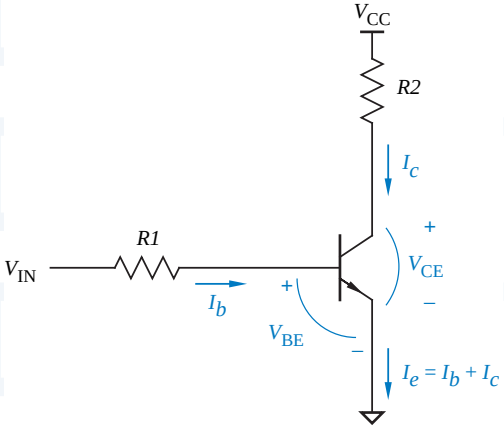


Figure 3-68
Common-emitter configuration of an *npn* transistor.

Copyright © 1999 by John F. Wakerly Copying Prohibited

Although the base current I_b controls the collector current flow I_c, it also indirectly controls the voltage V_{CE} across the collector-to-emitter junction, since V_{CE} is just the supply voltage V_{CC} minus the voltage drop across resistor *R2*:

$$\begin{aligned} V_{CE} &= V_{CC} - I_c \cdot R2 \\ &= V_{CC} - \beta \cdot I_b \cdot R2 \\ &= V_{CC} - (V_{IN} - 0.6) \cdot R2 / R1 \end{aligned}$$

However, in an ideal transistor V_{CE} can never be less than zero (the transistor cannot just create a negative potential), and in a real transistor V_{CE} can never be less than $V_{CE(sat)}$, a transistor parameter that is typically about 0.2 V.

If the values of V_{IN}, β, *R1*, and *R2* are such that the above equation predicts a value of V_{CE} that is less than $V_{CE(sat)}$, then the transistor cannot be operating in the active region and the equation does not apply. Instead, the transistor is operating in the *saturation region*, and is said to be *saturated (ON)*. No matter how much current I_b we put into the base, V_{CE} cannot drop below $V_{CE(sat)}$, and the collector current I_c is determined mainly by the load resistor *R2*:

saturation region

saturated (ON)

$$I_c = (V_{CC} - V_{CE(sat)}) / (R2 + R_{CE(sat)})$$

saturation resistance

Here, $R_{CE(sat)}$ is the *saturation resistance* of the transistor. Typically, $R_{CE(sat)}$ is 50 Ω or less and is insignificant compared with *R2*.

transistor simulation

Computer scientists might like to imagine an *npn* transistor as a device that continuously looks at its environment and executes the program in Table 3-10.

3.9.4 Transistor Logic Inverter

Figure 3-69 shows that we can make a logic inverter from an *npn* transistor in the common-emitter configuration. When the input voltage is LOW, the output voltage is HIGH, and vice versa.

In digital switching applications, bipolar transistors are often operated so they are always either cut off or saturated. That is, digital circuits such as the

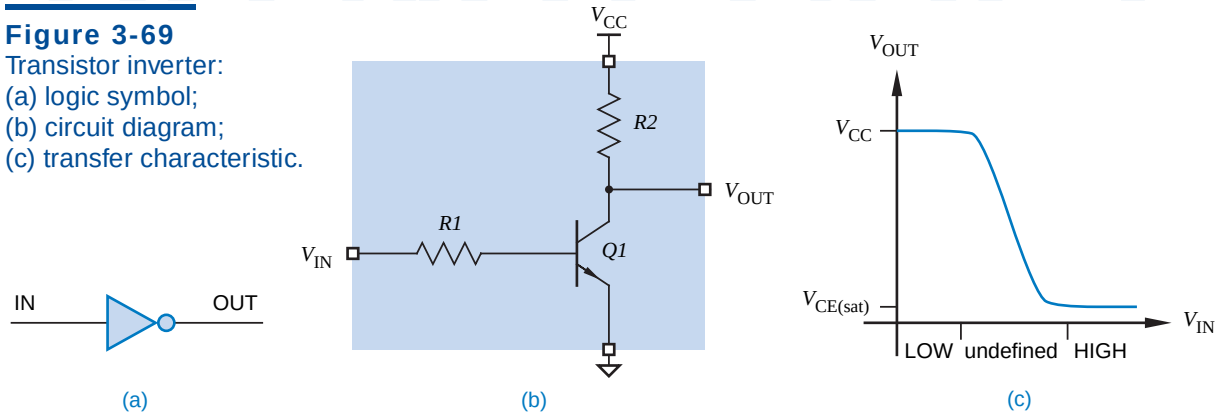


Figure 3-69
Transistor inverter:
(a) logic symbol;
(b) circuit diagram;
(c) transfer characteristic.

Copyright © 1999 by John F. Wakerly Copying Prohibited

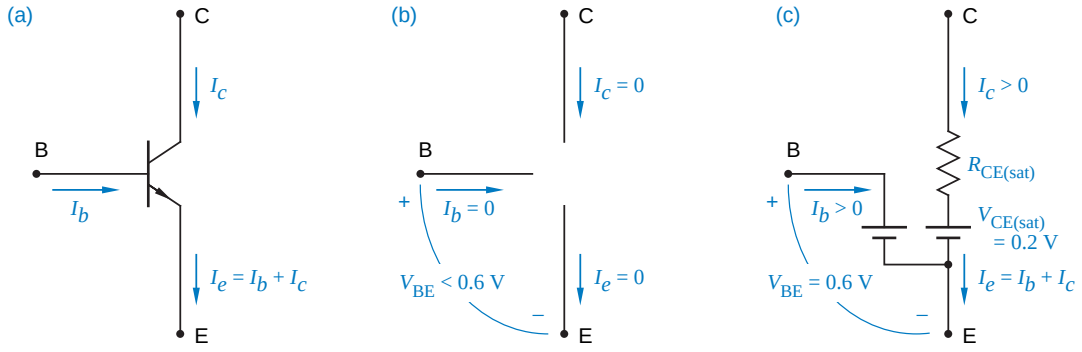
Table 3-10 A C program that simulates the function of an *npn* transistor in the common-emitter configuration.

```
/* Transistor parameters */
#define DIODEDROP 0.6 /* volts */
#define BETA 10;
#define VCE_SAT 0.2   /* volts */
#define RCE_SAT 50    /* ohms  */

main()
{
    float Vcc, Vin, R1, R2;  /* circuit parameters */
    float Ib, Ic, Vce;       /* circuit conditions */

    if (Vin < DIODEDROP) {   /* cut off */
       Ib  = 0.0;
       Ic  = 0.0;
       Vce = Vcc;
    }
    else {                   /* active or saturated */
        Ib = (Vin - DIODEDROP) / R1;
        if ((Vcc - ((BETA * Ib) * R2)) >= VCE_SAT) {   /* active */
           Ic  = BETA * Ib;
           Vce = Vcc - (Ic * R2);
        }
        else {               /* saturated */
           Vce = VCE_SAT;
           Ic  = (Vcc - Vce) / (R2 + RCE_SAT);
        }
    }
}
```

Figure 3-70 Normal states of an *npn* transistor in a digital switching circuit: (a) transistor symbol and currents; (b) equivalent circuit for a cut-off (OFF) transistor; (c) equivalent circuit for a saturated (ON) transistor.



Copyright © 1999 by John F. Wakerly Copying Prohibited

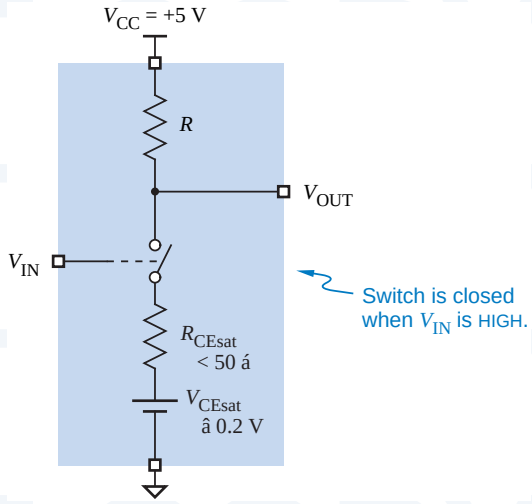


Figure 3-71
Switch model for a transistor inverter.

inverter in Figure 3-69 are designed so that their transistors are always (well, almost always) in one of the states depicted in Figure 3-70. When the input voltage V_{IN} is LOW, it is low enough that I_b is zero and the transistor is cut off; the collector-emitter junction looks like an open circuit. When V_{IN} is HIGH, it is high enough (and *R1* is low enough and β is high enough) that the transistor will be saturated for any reasonable value of *R2*; the collector-emitter junction looks almost like a short circuit. Input voltages in the undefined region between LOW and HIGH are not allowed, except during transitions. This undefined region corresponds to the noise margin that we discussed in conjunction with Table 3-1.

Another way to visualize the operation of a transistor inverter is shown in Figure 3-71. When V_{IN} is HIGH, the transistor switch is closed, and the output terminal is connected to ground, definitely a LOW voltage. When V_{IN} is LOW, the transistor switch is open and the output terminal is pulled to +5 V through a resistor; the output voltage is HIGH unless the output terminal is too heavily loaded (i.e., improperly connected through a low impedance to ground).

3.9.5 Schottky Transistors

storage time

When the input of a saturated transistor is changed, the output does not change immediately; it takes extra time, called *storage time*, to come out of saturation. In fact, storage time accounts for a significant portion of the propagation delay in the original TTL logic family.

Schottky diode
Schottky-clamped transistor
Schottky transistor

Storage time can be eliminated and propagation delay can be reduced by ensuring that transistors do not saturate in normal operation. Contemporary TTL logic families do this by placing a *Schottky diode* between the base and collector of each transistor that might saturate, as shown in Figure 3-72. The resulting transistors, which do not saturate, are called *Schottky-clamped transistors* or *Schottky transistors* for short.

Copyright © 1999 by John F. Wakerly Copying Prohibited

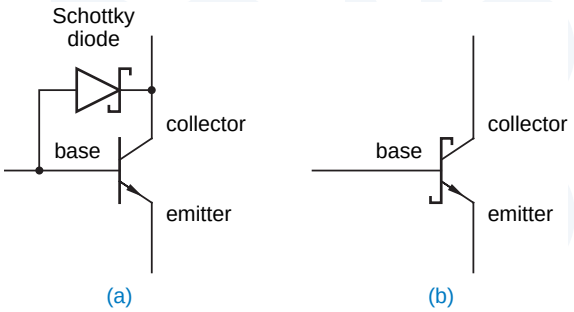


Figure 3-72
Schottky-clamped transistor: (a) circuit; (b) symbol.

When forward biased, a Schottky diode's voltage drop is much less than a standard diode's, 0.25 V vs. 0.6 V. In a standard saturated transistor, the base-to-collector voltage is 0.4 V, as shown in Figure 3-73(a). In a Schottky transistor, the Schottky diode shunts current from the base into the collector before the transistor goes into saturation, as shown in (b). Figure 3-74 is the circuit diagram of a simple inverter using a Schottky transistor.

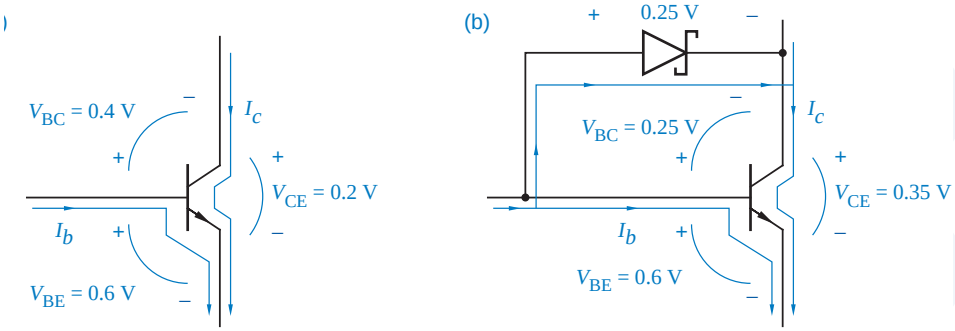


Figure 3-73 Operation of a transistor with large base current: (a) standard saturated transistor; (b) transistor with Schottky diode to prevent saturation.

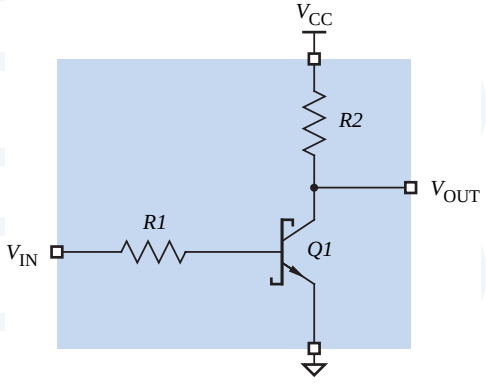


Figure 3-74
Inverter using Schottky transistor.

Copyright © 1999 by John F. Wakerly Copying Prohibited

3.10 Transistor-Transistor Logic

The most commonly used bipolar logic family is transistor-transistor logic. Actually, there are many different TTL families, with a range of speed, power consumption, and other characteristics. The circuit examples in this section are based on a representative TTL family, Low-power Schottky (LS or LS-TTL).

TTL families use basically the same logic levels as the TTL-compatible CMOS families in previous sections. We'll use the following definitions of LOW and HIGH in our discussions of TTL circuit behavior:

LOW 0–0.8 volts.
HIGH 2.0–5.0 volts.

3.10.1 Basic TTL NAND Gate

The circuit diagram for a two-input LS-TTL NAND gate, part number 74LS00, is shown in Figure 3-75. The NAND function is obtained by combining a diode AND gate with an inverting buffer amplifier. The circuit's operation is best understood by dividing it into the three parts that are shown in the figure and discussed in the next three paragraphs:

- Diode AND gate and input protection.
- Phase splitter.
- Output stage.

diode AND gate
clamp diode

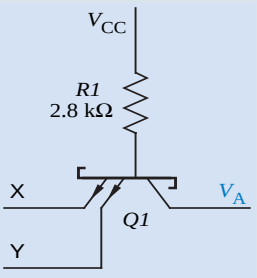
Diodes *D1X* and *D1Y* and resistor *R1* in Figure 3-75 form a *diode AND gate*, as in Section 3.9.2. *Clamp diodes D2X* and *D2Y* do nothing in normal operation, but limit undesirable negative excursions on the inputs to a single diode drop. Such negative excursions may occur on HIGH-to-LOW input transitions as a result of transmission-line effects, discussed in Section 12.4.

phase splitter

Transistor *Q2* and the surrounding resistors form a *phase splitter* that controls the output stage. Depending on whether the diode AND gate produces a "low" or a "high" voltage at V_A, *Q2* is either cut off or turned on.

WHERE IN THE WORLD IS *Q1*?

Notice that there is no transistor *Q1* in Figure 3-75, but the other transistors are named in a way that's traditional; some TTL devices do in fact have a transistor named *Q1*. Instead of diodes like *D1X* and *D1Y*, these devices use a multiple-emitter transistor *Q1* to perform logic. This transistor has one emitter per logic input, as shown in the figure to the right. Pulling any one of the emitters LOW is sufficient to turn the transistor ON and thus pull V_A LOW.



Copyright © 1999 by John F. Wakerly Copying Prohibited

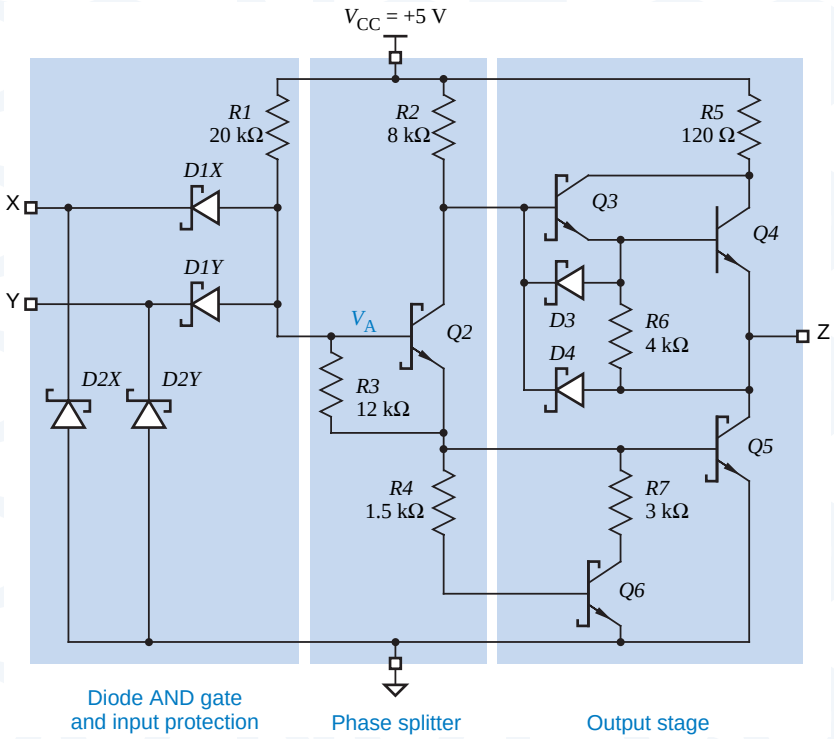


Figure 3-75
Circuit diagram of two-input LS-TTL NAND gate.

The *output stage* has two transistors, *Q4* and *Q5*, only one of which is on at any time. The TTL output stage is sometimes called a *totem-pole* or *push-pull output*. Similar to the *p*-channel and *n*-channel transistors in CMOS, *Q4* and *Q5* provide active pull-up and pull-down to the HIGH and LOW states, respectively.

output stage
totem-pole output
push-pull output

The functional operation of the TTL NAND gate is summarized in Figure 3-76(a). The gate does indeed perform the NAND function, with the truth table and logic symbol shown in (b) and (c). TTL NAND gates can be designed with any desired number of inputs simply by changing the number of diodes in

(a)

X	Y	V_A	*Q2*	*Q3*	*Q4*	*Q5*	*Q6*	V_Z	Z
L	L	≤1.05	off	on	on	off	off	2.7	H
L	H	≤1.05	off	on	on	off	off	2.7	H
H	L	≤1.05	off	on	on	off	off	2.7	H
H	H	1.2	on	off	off	on	on	≤0.35	L

(b)

X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

(c)

Figure 3-76
Functional operation of a TTL two-input NAND gate:
(a) function table;
(b) truth table;
(c) logic symbol.

Copyright © 1999 by John F. Wakerly Copying Prohibited

the diode AND gate in the figure. Commercially available TTL NAND gates have as many as 13 inputs. A TTL inverter is designed as a 1-input NAND gate, omitting diodes *D1Y* and *D2Y* in Figure 3-75.

Since the output transistors *Q4* and *Q5* are normally complementary—one ON and the other OFF—you might question the purpose of the 120 Ω resistor *R5* in the output stage. A value of 0 Ω would give even better driving capability in the HIGH state. This is certainly true from a DC point of view. However, when the TTL output is changing from HIGH to LOW or vice versa, there is a short time when both transistors may be on. The purpose of *R5* is to limit the amount of current that flows from VCC to ground during this time. Even with a 120 Ω resistor in the TTL output stage, higher-than-normal currents called current spikes flow when TTL outputs are switched. These are similar to the current spikes that occur when high-speed CMOS outputs switch.

So far we have shown the input signals to a TTL gate as ideal voltage sources. Figure 3-77 shows the situation when a TTL input is driven LOW by the output of another TTL gate. Transistor *Q5A* in the driving gate is ON, and thereby provides a path to ground for the current flowing out of the diode *D1XB* in the driven gate. When current flows *into* a TTL output in the LOW state, as in this case, the output is said to be *sinking current*.

sinking current

Figure 3-78 shows the same circuit with a HIGH output. In this case, *Q4A* in the driving gate is turned on enough to supply the small amount of leakage current flowing through reverse-biased diodes *D1XB* and *D2XB* in the driven gate. When current flows out of a TTL output in the HIGH state, the output is said to be *sourcing current*.

sourcing current

3.10.2 Logic Levels and Noise Margins

At the beginning of this section, we indicated that we would consider TTL signals between 0 and 0.8 V to be LOW, and signals between 2.0 and 5.0 V to be HIGH. Actually, we can be more precise by defining TTL input and output levels in the same way as we did for CMOS:

V_{OHmin} The minimum output voltage in the HIGH state, 2.7 V for most TTL families.

V_{IHmin} The minimum input voltage guaranteed to be recognized as a HIGH, 2.0 V for all TTL families.

CURRENT SPIKES AGAIN

Current spikes can show up as noise on the power-supply and ground connections in TTL and CMOS circuits, especially when multiple outputs are switched simultaneously. For this reason, reliable circuits require decoupling capacitors between V_{CC} and ground, distributed throughout the circuit so that there is a capacitor within an inch or so of each chip. Decoupling capacitors supply the instantaneous current needed during transitions.

Copyright © 1999 by John F. Wakerly Copying Prohibited

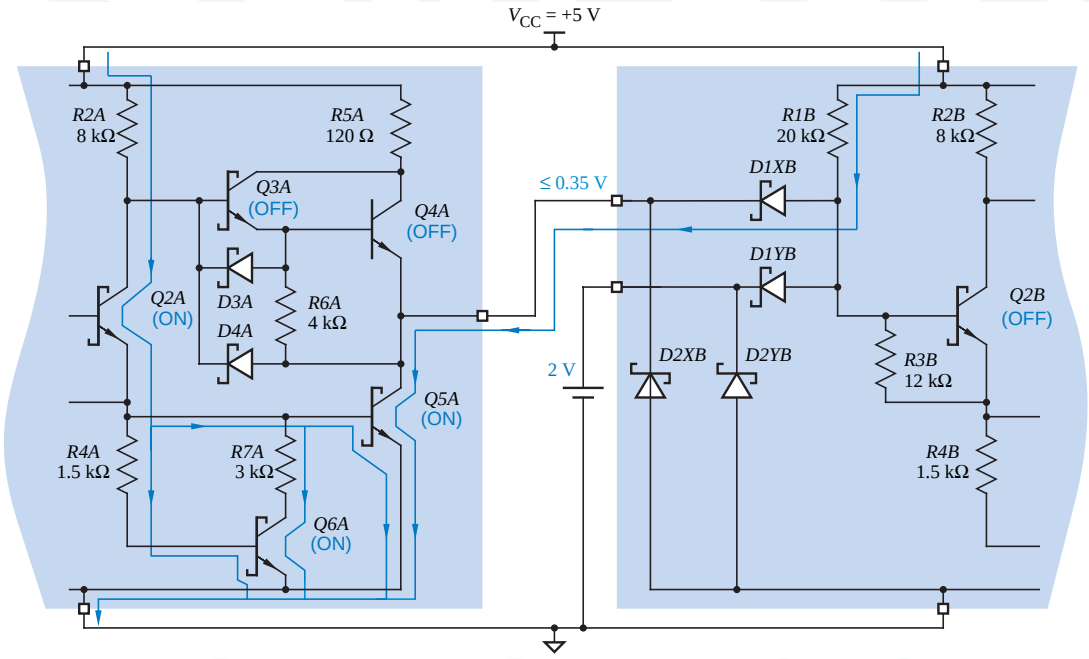


Figure 3-77 A TTL output driving a TTL input LOW.

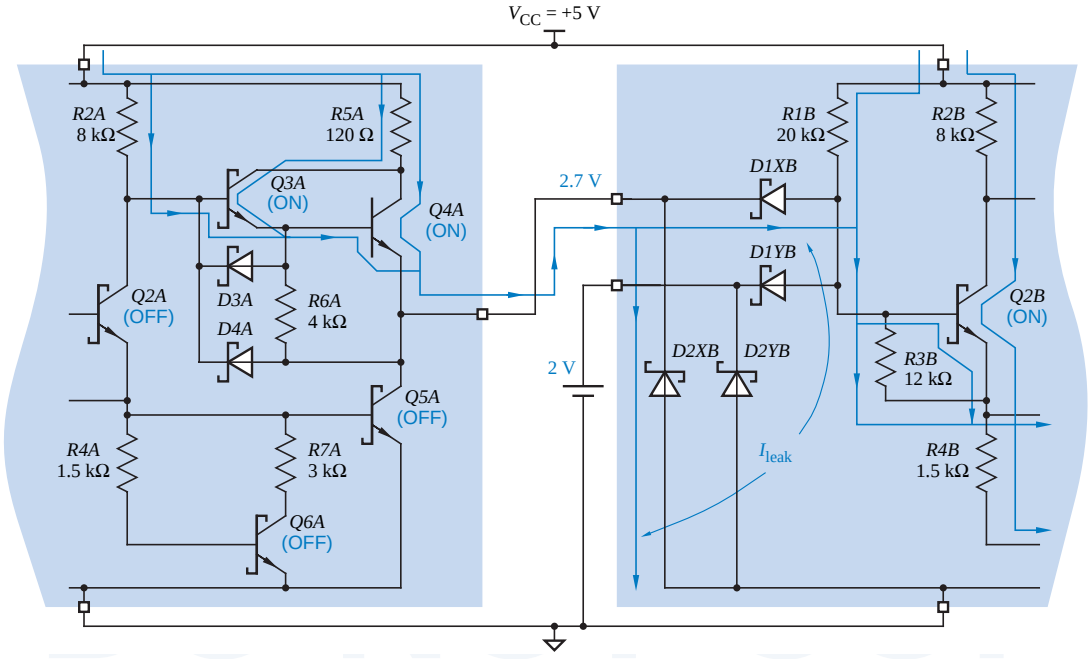


Figure 3-78 A TTL output driving a TTL input HIGH.

Copyright © 1999 by John F. Wakerly Copying Prohibited

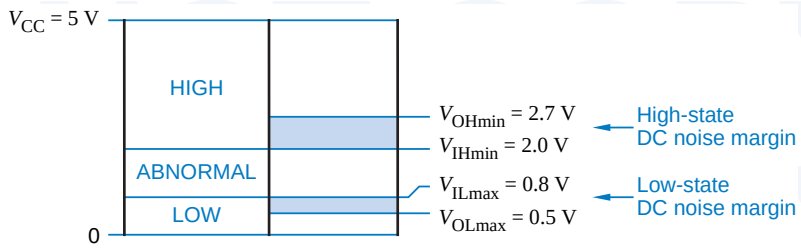


Figure 3-79
Noise margins for popular TTL logic families (74LS, 74S, 74ALS, 74AS, 74F).

V_{ILmax} The maximum input voltage guaranteed to be recognized as a LOW, 0.8 V for most TTL families.

V_{OLmax} The maximum output voltage in the LOW state, 0.5 V for most families.

These noise margins are illustrated in Figure 3-79.

DC noise margin

In the HIGH state, the V_{OHmin} specification of most TTL families exceeds V_{IHmin} by 0.7 V, so TTL has a *DC noise margin* of 0.7 V in the HIGH state. That is, it takes at least 0.7 V of noise to corrupt a worst-case HIGH output into a voltage that is not guaranteed to be recognizable as a HIGH input. In the LOW state, however, V_{ILmax} exceeds V_{OLmax} by only 0.3 V, so the DC noise margin in the LOW state is only 0.3 V. In general, TTL and TTL-compatible circuits tend to be more sensitive to noise in the LOW state than in the HIGH state.

3.10.3 Fanout

fanout

As we defined it previously in Section 3.5.4, *fanout* is a measure of the number of gate inputs that are connected to (and driven by) a single gate output. As we showed in that section, the DC fanout of CMOS outputs driving CMOS inputs is virtually unlimited, because CMOS inputs require almost no current in either state, HIGH or LOW. This is not the case with TTL inputs. As a result, there are very definite limits on the fanout of TTL or CMOS outputs driving TTL inputs, as you'll learn in the paragraphs that follow.

current flow

As in CMOS, the *current flow* in a TTL input or output lead is defined to be positive if the current actually flows *into* the lead, and negative if current flows *out* of the lead. As a result, when an output is connected to one or more inputs, the algebraic sum of all the input and output currents is 0.

The amount of current required by a TTL input depends on whether the input is HIGH or LOW, and is specified by two parameters:

I_{ILmax} The maximum current that an input requires to pull it LOW. Recall from the discussion of Figure 3-77 that positive current is actually flowing from V_{CC}, through *R1B*, through diode *D1XB*, out of the input lead, through the driving output transistor *Q5A*, and into ground.

Since current flows out of a TTL input in the LOW state, I_{ILmax} has a negative value. Most LS-TTL inputs have $I_{ILmax} = -0.4$ mA, which is sometimes called a *LOW-state unit load* for LS-TTL.

LOW-state unit load

Copyright © 1999 by John F. Wakerly Copying Prohibited

I_{IHmax} The maximum current that an input requires to pull it HIGH. As shown in Figure 3-78 on page 155, positive current flows from V_{CC}, through *R5A* and *Q4A* of the driving gate, and *into* the driven input, where it leaks to ground through reversed-biased diodes *D1XB* and *D2XB*.

Since current flows *into* a TTL input in the HIGH state, I_{IHmax} has a positive value. Most LS-TTL inputs have I_{IHmax} = 20 μA, which is sometimes called a *HIGH-state unit load* for LS-TTL.

HIGH-state unit load

Like CMOS outputs, TTL outputs can source or sink a certain amount of current depending on the state, HIGH or LOW:

I_{OLmax} The maximum current an output can sink in the LOW state while maintaining an output voltage no more than V_{OLmax}. Since current flows into the output, I_{OLmax} has a positive value, 8 mA for most LS-TTL outputs.

I_{OHmax} The maximum current an output can source in the HIGH state while maintaining an output voltage no less than V_{OHmin}. Since current flows out of the output, I_{OHmax} has a negative value, −400 μA for most LS-TTL outputs.

Notice that the value of I_{OLmax} for typical LS-TTL outputs is exactly 20 times the absolute value of I_{ILmax}. As a result, LS-TTL is said to have a *LOW-state fanout* of 20, because an output can drive up to 20 inputs in the LOW state. Similarly, the absolute value of I_{OHmax} is exactly 20 times I_{IHmax}, so LS-TTL is said to have a *HIGH-state fanout* of 20 also. The *overall fanout* is the lesser of the LOW- and HIGH-state fanouts.

LOW-state fanout

HIGH-state fanout

overall fanout

Loading a TTL output with more than its rated fanout has the same deleterious effects that were described for CMOS devices in Section 3.5.5 on page 106. That is, DC noise margins may be reduced or eliminated, transition times and delays may increase, and the device may overheat.

TTL OUTPUT ASYMMETRY

Although LS-TTL's numerical fanouts for HIGH and LOW states are equal, LS-TTL and other TTL families have a definite asymmetry in current driving capability—an LS-TTL output can sink 8 mA in the LOW state, but can source only 400 μA in the HIGH state.

This asymmetry is no problem when TTL outputs drive other TTL inputs, because it is matched by a corresponding asymmetry in TTL input current requirements (I_{ILmax} is large, while I_{IHmax} is small). However, it is a limitation when TTL is used to drive LEDs, relays, solenoids, or other devices requiring large amounts of current, often tens of milliamperes. Circuits using these devices must be designed so that current flows (and the driven device is "on") when the TTL output is in the LOW state, and so little or no current flows in the HIGH state. Special TTL buffer/driver gates are made that can sink up to 60 mA in the LOW state, but that still have a rather puny current sourcing capability in the HIGH state (2.4 mA).

Copyright © 1999 by John F. Wakerly Copying Prohibited

BURNED FINGERS If a TTL or CMOS output is forced to sink a lot more than I_{OLmax}, the device may be damaged, especially if high current is allowed to flow for more than a second or so. For example, suppose that a TTL output in the LOW state is short-circuited directly to the 5 V supply. The ON resistance, $R_{CE(sat)}$, of the saturated *Q5* transistor in a typical TTL output stage is less than 10 Ω. Thus, *Q5* must dissipate about $5^2/10$ or 2.5 watts. Don't try this yourself unless you're prepared to deal with the consequences! That's enough heat to destroy the device (and burn your finger) in a very short time.

In general, two calculations must be carried out to confirm that an output is not being overloaded:

HIGH state The I_{IHmax} values for all of the driven inputs are added. This sum must be less than or equal to the absolute value of I_{OHmax} for the driving output.

LOW state The I_{ILmax} values for all of the driven inputs are added. The absolute value of this sum must be less than or equal to I_{OLmax} for the driving output.

For example, suppose you designed a system in which a certain LS-TTL output drives ten LS-TTL and three S-TTL gate inputs. In the HIGH state, a total of $10 \cdot 20 + 3 \cdot 50\ \mu A = 350\ \mu A$ is required. This is within an LS-TTL output's HIGH-state current-sourcing capability of 400 μA. But in the LOW state, a total of $10 \cdot 0.4 + 3 \cdot 2.0$ mA = 10.0 mA is required. This is more than an LS-TTL output's LOW-state current-sinking capability of 8 mA, so the output is overloaded.

3.10.4 Unused Inputs

Unused inputs of TTL gates can be handled in the same way as we described for CMOS gates in Section 3.5.6 on page 107. That is, unused inputs may be tied to used ones, or unused inputs may be pulled HIGH or LOW as is appropriate for the logic function.

The resistance value of a pull-up or pull-down resistor is more critical with TTL gates than CMOS gates, because TTL inputs draw significantly more current, especially in the LOW state. If the resistance is too large, the voltage drop across the resistor may result in a gate input voltage beyond the normal LOW or HIGH range.

For example, consider the pull-down resistor shown in Figure 3-80. The pull-down resistor must sink 0.4 mA of current from each of the unused LS-TTL inputs that it drives. Yet the voltage drop across the resistor must be no more than 0.5 V in order to have a LOW input voltage no worse than that produced by a normal gate output. If the resistor drives *n* LS-TTL inputs, then we must have

$$n \cdot 0.4\ \text{mA} \cdot R_{pd} < 0.5\ \text{V}$$

Copyright © 1999 by John F. Wakerly Copying Prohibited

FLOATING TTL INPUTS

Analysis of the TTL input structure shows that unused inputs left unconnected (or *floating*) behave as if they have a HIGH voltage applied—they are pulled HIGH by base resistor *R1* in Figure 3-75 on page 153. However, *R1*'s pull-up is much weaker than that of a TTL output driving the input. As a result, a small amount of circuit noise, such as that produced by other gates when they switch, can make a floating input spuriously behave like it's LOW. Therefore, for the sake of reliability, unused TTL inputs should be tied to a stable HIGH or LOW voltage source.

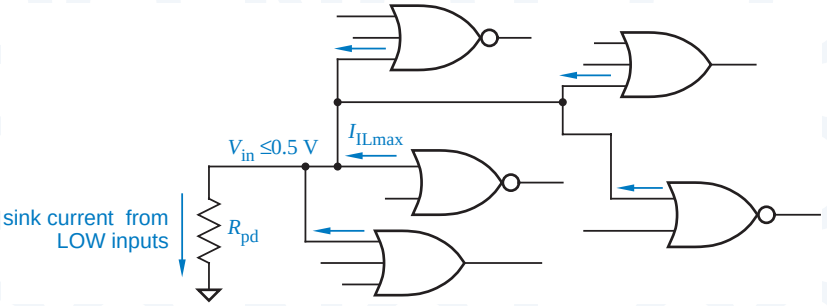


Figure 3-80
Pull-down resistor for TTL inputs.

Thus, if the resistor must pull 10 LS-TTL inputs LOW, then we must have $R_{pd} < 0.5 / (10 \cdot 4 \cdot 10^{-3})$, or $R_{pd} < 125\ \Omega$.

Similarly, consider the pull-up resistor shown in Figure 3-81. It must source 20 μA of current to each unused input while producing a HIGH voltage no worse than that produced by a normal gate output, 2.7 V. Therefore, the voltage drop across the resistor must be no more than 2.3 V; if *n* LS-TTL input are driven, we must have

$$n \cdot 20\ \mu A \cdot R_{pu} < 2.3\ \text{V}$$

Thus, if 10 LS-TTL inputs are pulled up, then $R_{pu} < 2.3 / (10 \cdot 20 \cdot 10^{-6})$, or $R_{pu} < 11.5\ \text{K}\Omega$.

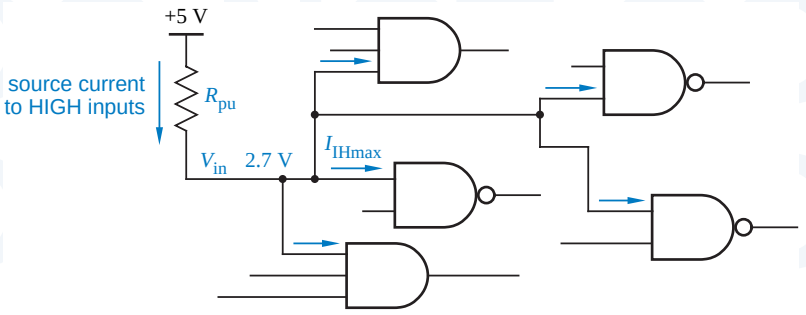


Figure 3-81
Pull-up resistor for TTL inputs.

Copyright © 1999 by John F. Wakerly Copying Prohibited

WHY USE A RESISTOR?

You might be asking yourself, "Why use a pull-up or pull-down resistor, when a direct connection to ground or the 5-V power supply should be a perfectly good source of LOW or HIGH?"

Well, for a HIGH source, a direct connection to the 5 V power supply is not recommended, since an input transient of over 5.5 V can damage some TTL devices, ones that use a multi-emitter transistor in the input stage. The pull-up resistor limits current and prevents damage in this case.

For a LOW source, a direct connection to ground without the pull-down resistor is actually OK in most cases. You'll see many examples of this sort of connection throughout this book. However, as explained in Section 12.2.2 on page 803, the pull-down resistor is still desirable in some cases so that the "constant" LOW signal it produces can be overridden and driven HIGH for system-testing purposes.

3.10.5 Additional TTL Gate Types

Although the NAND gate is the "workhorse" of the TTL family, other types of gates can be built with the same general circuit structure.

The circuit diagram for an LS-TTL NOR gate is shown in Figure 3-82. If either input X or Y is HIGH, the corresponding phase-splitter transistor *Q2X* or *Q2Y* is turned on, which turns off *Q3* and *Q4* while turning on *Q5* and *Q6*, and the output is LOW. If both inputs are LOW, then both phase-splitter transistors are off, and the output is forced HIGH. This functional operation is summarized in Figure 3-83.

The LS-TTL NOR gate's input circuits, phase splitter, and output stage are almost identical to those of an LS-TTL NAND gate. The difference is that an LS-TTL NAND gate uses diodes to perform the AND function, while an LS-TTL NOR gate uses parallel transistors in the phase splitter to perform the OR function.

The speed, input, and output characteristics of a TTL NOR gate are comparable to those of a TTL NAND. However, an *n*-input NOR gate uses more transistors and resistors and is thus more expensive in silicon area than an *n*-input NAND. Also, internal leakage current limits the number of *Q2* transistors that can be placed in parallel, so NOR gates have poor fan-in. (The largest discrete TTL NOR gate has only 5 inputs, compared with a 13-input NAND.) As a result, NOR gates are less commonly used than NAND gates in TTL designs.

The most "natural" TTL gates are inverting gates like NAND and NOR. Noninverting TTL gates include an extra inverting stage, typically between the input stage and the phase splitter. As a result, noninverting TTL gates are typically larger and slower than the inverting gates on which they are based.

Like CMOS, TTL gates can be designed with three-state outputs. Such gates have an "output-enable" or "output-disable" input that allows the output to be placed in a high-impedance state where neither output transistor is turned on.

Copyright © 1999 by John F. Wakerly Copying Prohibited

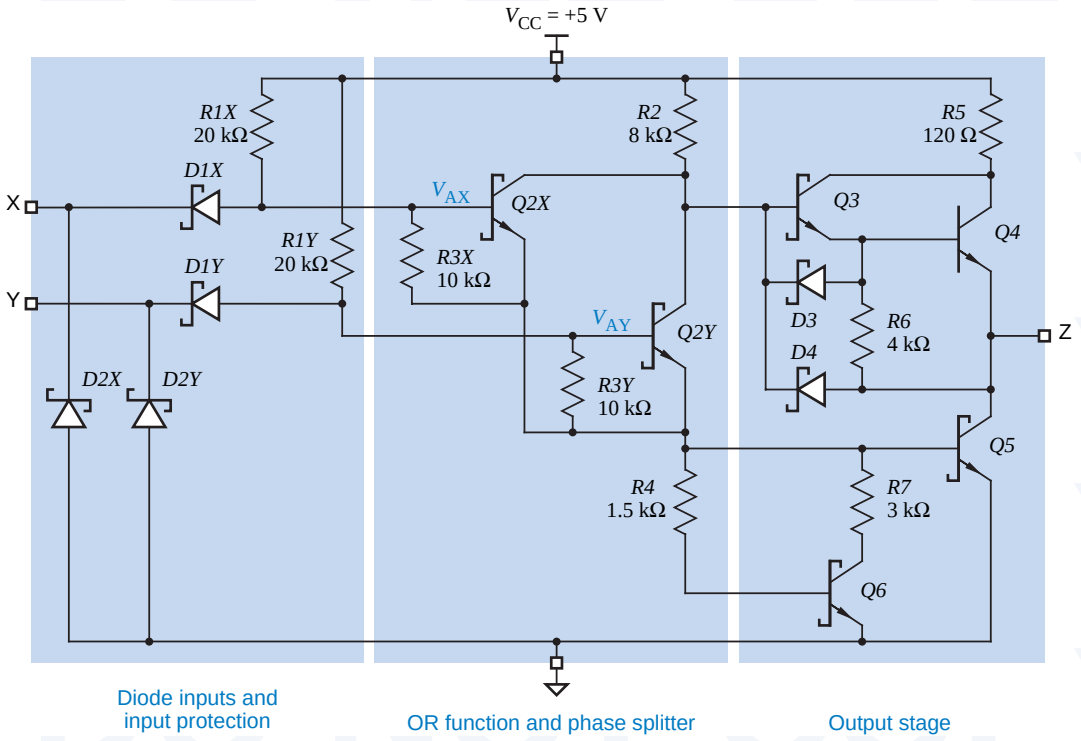


Figure 3-82 Circuit diagram of a two-input LS-TTL NOR gate.

(a)

X	Y	V_{AX}	Q2X	V_{AY}	Q2Y	Q3	Q4	Q5	Q6	V_Z	Z
L	L	≤1.05	off	≤1.05	off	on	on	off	off	≥2.7	H
L	H	≤1.05	off	1.2	on	off	off	on	on	≤0.35	L
H	L	1.2	on	≤1.05	off	off	off	on	on	≤0.35	L
H	H	1.2	on	1.2	on	off	off	on	on	≤0.35	L

(b)

X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

(c)

Figure 3-83 Two-input LS-TTL NOR gate: (a) function table; (b) truth table; (c) logic symbol.

Some TTL gates are also available with *open-collector outputs*. Such gates omit the entire upper half of the output stage in Figure 3-75, so that only passive pull-up to the HIGH state is provided by an external resistor. The applications and required calculations for TTL open-collector gates are similar to those for CMOS gates with open-drain outputs.

open-collector output

Copyright © 1999 by John F. Wakerly Copying Prohibited

3.11 TTL Families

TTL families have evolved over the years in response to the demands of digital designers for better performance. As a result, three TTL families have come and gone, and today's designers have five surviving families from which to choose. All of the TTL families are compatible in that they use the same power supply voltage and logic levels, but each family has its own advantages in terms of speed, power consumption, and cost.

3.11.1 Early TTL Families

The original TTL family of logic gates was introduced by Sylvania in 1963. It was popularized by Texas Instruments, whose "7400-series" part numbers for gates and other TTL components quickly became an industry standard.

As in 7400-series CMOS, devices in a given TTL family have part numbers of the form 74FAM*nn*, where "FAM" is an alphabetic family mnemonic and *nn* is a numeric function designator. Devices in different families with the same value of *nn* perform the same function. In the original TTL family, "FAM" is null and the family is called *74-series TTL*.

74-series TTL

Resistor values in the original TTL circuit were changed to obtain two more TTL families with different performance characteristics. The *74H (High-speed TTL)* family used lower resistor values to reduce propagation delay at the expense of increased power consumption. The *74L (Low-power TTL)* family used higher resistor values to reduce power consumption at the expense of propagation delay.

74H (High-speed TTL)

74L (Low-power TTL)

The availability of three TTL families allowed digital designers in the 1970s to make a choice between high speed and low power consumption for their circuits. However, like many people in the 1970s, they wanted to "have it all, now." The development of Schottky transistors provided this opportunity, and made 74, 74H, and 74L TTL obsolete. The characteristics of better-performing, contemporary TTL families are discussed in the rest of this section.

3.11.2 Schottky TTL Families

Historically, the first family to make use of Schottky transistors was *74S (Schottky TTL)*. With Schottky transistors and low resistor values, this family has much higher speed, but higher power consumption, than the original 74-series TTL.

74S (Schottky TTL)

Perhaps the most widely used and certainly the least expensive TTL family is *74LS (Low-power Schottky TTL)*, introduced shortly after 74S. By combining Schottky transistors with higher resistor values, 74LS TTL matches the speed of 74-series TTL but has about one-fifth of its power consumption. Thus, 74LS is a preferred logic family for new TTL designs.

74LS (Low-power Schottky TTL)

Subsequent IC processing and circuit innovations gave rise to two more Schottky logic families. The *74AS (Advanced Schottky TTL)* family offers speeds approximately twice as fast as 74S with approximately the same power

74AS (Advanced Schottky TTL)

Copyright © 1999 by John F. Wakerly Copying Prohibited

Table 3-11 Characteristics of gates in TTL families.

Description	Symbol	Family				
		74S	74LS	74AS	74ALS	74F
Maximum propagation delay (ns)		3	9	1.7	4	3
Power consumption per gate (mW)		19	2	8	1.2	4
Speed-power product (pJ)		57	18	13.6	4.8	12
LOW-level input voltage (V)	V_{ILmax}	0.8	0.8	0.8	0.8	0.8
LOW-level output voltage (V)	V_{OLmax}	0.5	0.5	0.5	0.5	0.5
HIGH-level input voltage (V)	V_{IHmin}	2.0	2.0	2.0	2.0	2.0
HIGH-level output voltage (V)	V_{OHmin}	2.7	2.7	2.7	2.7	2.7
LOW-level input current (mA)	I_{ILmax}	–2.0	–0.4	–0.5	–0.2	–0.6
LOW-level output current (mA)	I_{OLmax}	20	8	20	8	20
HIGH-level input current (μA)	I_{IHmax}	50	20	20	20	20
HIGH-level output current (μA)	I_{OHmax}	–1000	–400	–2000	–400	–1000

consumption. The *74ALS (Advanced Low-power Schottky TTL)* family offers both lower power and higher speeds than 74LS, and rivals 74LS in popularity for general-purpose requirements in new TTL designs. The *74F (Fast TTL)* family is positioned between 74AS and 74ALS in the speed/power tradeoff, and is probably the most popular choice for high-speed requirements in new TTL designs.

74ALS (Advanced Low-power Schottky TTL)

74F (Fast TTL)

3.11.3 Characteristics of TTL Families

The important characteristics of contemporary TTL families are summarized in Table 3-11. The first two rows of the table list the propagation delay (in nanoseconds) and the power consumption (in milliwatts) of a typical 2-input NAND gate in each family.

One figure of merit of a logic family is its *speed-power product* listed in the third row of the table. As discussed previously, this is simply the product of the propagation delay and power consumption of a typical gate. The speed-power product measures a sort of efficiency—how much energy a logic gate uses to switch its output.

The remaining rows in Table 3-11 describe the input and output parameters of typical TTL gates in each of the families. Using this information, you can

Copyright © 1999 by John F. Wakerly Copying Prohibited

analyze the external behavior of TTL gates without knowing the details of the internal TTL circuit design. These parameters were defined and discussed in Sections 3.10.2 and 3.10.3. As always, the input and output characteristics of specific components may vary from the representative values given in Table 3-11, so you must always consult the manufacturer's data book when analyzing a real design.

3.11.4 A TTL Data Sheet

Table 3-12 shows the part of a typical manufacturer's data sheet for the 74LS00. The 54LS00 listed in the data sheet is identical to the 74LS00, except that it is specified to operate over the full "military" temperature and voltage range, and it costs more. Most TTL parts have corresponding 54-series (military) versions. Three sections of the data sheet are shown in the table:

recommended operating conditions

- *Recommended operating conditions* specify power-supply voltage, input-voltage ranges, DC output loading, and temperature values under which the device is normally operated.

electrical characteristics

- *Electrical characteristics* specify additional DC voltages and currents that are observed at the device inputs and output when it is operated under the recommended conditions:

  I_I Maximum input current for a very high HIGH input voltage.

  I_{OS} Output current with HIGH output shorted to ground.

  I_{CCH} Power-supply current when all outputs (on four NAND gates) are HIGH. (The number given is for the entire package, which contains four NAND gates, so the current per gate is one-fourth of the specified amount.)

  I_{CCL} Power-supply current when all outputs (on four NAND gates) are LOW.

switching characteristics

- *Switching characteristics* give maximum and typical propagation delays under "typical" operating conditions of $V_{CC} = 5$ V and $T_A = 25°C$. A conservative designer must increase these delays by 5%–10% to account for different power-supply voltages and temperatures, and even more under heavy loading conditions.

A fourth section is also included in the manufacturer's data book:

absolute maximum ratings

- *Absolute maximum ratings* indicate the worst-case conditions for operating or storing the device without damage.

A complete data book also shows test circuits that are used to measure the parameters when the device is manufactured, and graphs that show how the typical parameters vary with operating conditions such as power-supply voltage (V_{CC}), ambient temperature (T_A), and load (R_L, C_L).

Copyright © 1999 by John F. Wakerly Copying Prohibited

Table 3-12 Typical manufacturer's data sheet for the 74LS00.

RECOMMENDED OPERATING CONDITIONS

		SN54LS00			SN74LS00			
Parameter	***Description***	***Min.***	***Nom.***	***Max.***	***Min.***	***Nom.***	***Max.***	***Unit***
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			4			4	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED FREE-AIR TEMPERATURE RANGE

		SN54LS00			SN74LS00			
Parameter	***Test Conditions*[1]**	***Min.***	***Typ.*[2]**	***Max.***	***Min.***	***Typ.*[2]**	***Max.***	***Unit***
V_{IK}	V_{CC} = Min., I_N = –18 mA			–1.5			–1.5	V
V_{OH}	V_{CC} = Min., V_{IL} = Max., I_{OH} = –0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = Min., V_{IH} = 2.0 V, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = Min., V_{IH} = 2.0 V, I_{OL} = 8 mA					0.35		
I_I	V_{CC} = Max., V_I = 7.0 V			0.1			0.1	mA
I_{IH}	V_{CC} = Max. V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = Max. V_I = 0.4 V			–0.4			–0.4	mA
I_{IOS}[3]	V_{CC} = Max.	–20		–100	–20		–100	mA
I_{CCH}	V_{CC} = Max., V_I = 0 V		0.8	1.6		0.8	1.6	mA
I_{CCL}	V_{CC} = Max., V_I = 4.5 V		2.4	4.4		2.4	4.4	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5.0 V, T_A = 25°C

DO NOT COPY

Copyright © 1999 by John F. Wakerly Copying Prohibited

stantial current, especially compared to HC and HCT output capabilities. For example, an HC or HCT output can drive 10 LS or only two S-TTL inputs.

The last factor is capacitive loading. We've seen that load capacitance increases both the delay and the power dissipation of logic circuits. Increases in delay are especially noticeable with HC and HCT outputs, whose transition times increase about 1 ns for each 5 pF of load capacitance. The transistors in FCT outputs have very low "on" resistances, so their transition times increase only about 0.1 ns for each 5 pF of load capacitance.

For a given load capacitance, power-supply voltage, and application, all of the CMOS families have similar dynamic power dissipation, since each variable in the CV^2f equation is the same. On the other hand, TTL outputs have somewhat lower dynamic power dissipation, since the voltage swing between TTL HIGH and LOW levels is smaller.

*3.13 Low-Voltage CMOS Logic and Interfacing

Two important factors have led the IC industry to move towards lower power-supply voltages in CMOS devices:

- In most applications, CMOS output voltages swing from rail to rail, so the V in the CV^2f equation is the power-supply voltage. Cutting power-supply voltage reduces dynamic power dissipation more than proportionally.
- As the industry moves towards ever-smaller transistor geometries, the oxide insulation between a CMOS transistor's gate and its source and drain is getting ever thinner, and thus incapable of insulating voltage potentials as "high" as 5 V.

As a result, JEDEC, an IC industry standards group, selected $3.3\,V \pm 0.3V$, $2.5\,V \pm 0.2V$, and $1.8\,V \pm 0.15V$ as the next "standard" logic power-supply voltages. JEDEC standards specify the input and output logic voltage levels for devices operating with these power-supply voltages.

The migration to lower voltages has occurred in stages, and will continue to do so. For discrete logic families, the trend has been to produce parts that operate and produce outputs at the lower voltage, but that can also tolerate inputs at the higher voltage. This approach has allowed 3.3-V CMOS families to operate with 5-V CMOS and TTL families, as we'll see in the next section.

Many ASICs and microprocessors have followed a similar approach, but another approach is often used as well. These devices are large enough that it can make sense to provide them with two power-supply voltages. A low voltage, such as 2.5 V, is supplied to operate the chip's internal gates, or *core logic*. A higher voltage, such as 3.3 V, is supplied to operate the external input and output circuits, or *pad ring*, for compatibility with older-generation devices in the system. Special buffer circuits are used internally to translate safely and quickly between the core-logic and the pad-ring logic voltages.

core logic

pad ring

Copyright © 1999 by John F. Wakerly Copying Prohibited

*3.13.1 3.3-V LVTTL and LVCMOS Logic

The relationships among signal levels for standard TTL and low-voltage CMOS devices operating at their nominal power-supply voltages are illustrated nicely in Figure 3-85, adapted from a Texas Instruments application note. The original, symmetric signal levels for pure 5-V CMOS families such as HC and VHC are shown in (a). TTL-compatible CMOS families such as HCT, VHCT, and FCT shift the voltage levels downwards for compatibility with TTL as shown in (b).

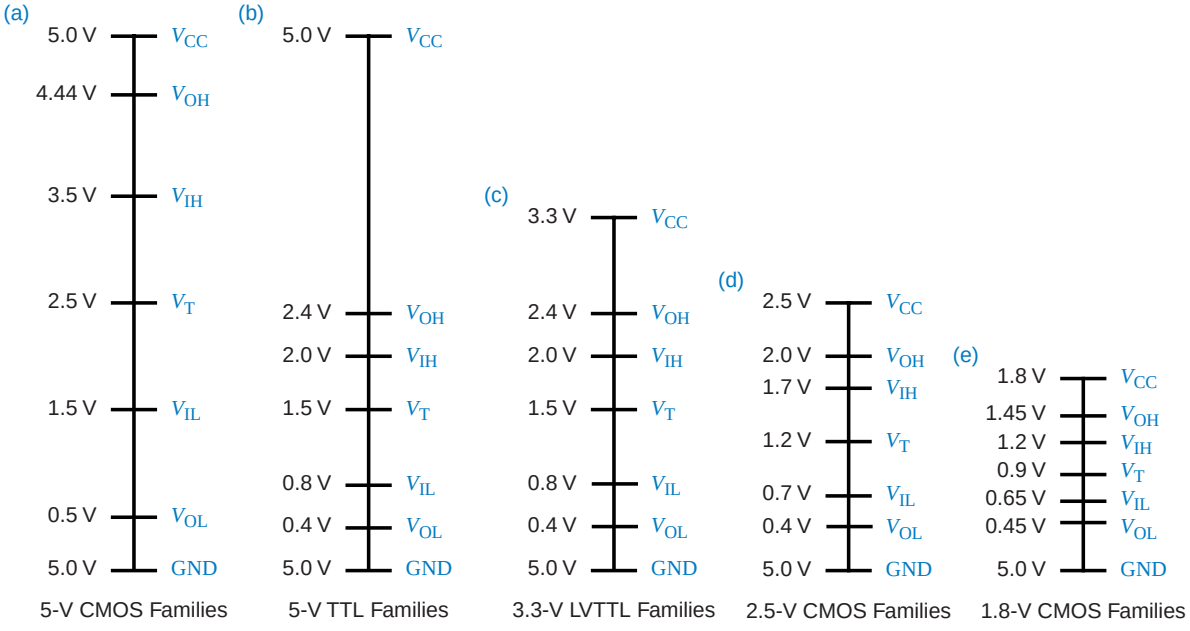
The first step in the progression of lower CMOS power-supply voltages was 3.3 V. The JEDEC standard for 3.3-V logic actually defines two sets of levels. *LVCMOS (low-voltage CMOS)* levels are used in pure CMOS applications where outputs have light DC loads (less than 100 μA), so V_{OL} and V_{OH} are maintained within 0.2 V of the power-supply rails. *LVTTL (low-voltage TTL)* levels, shown in (c), are used in applications where outputs have significant DC loads, so V_{OL} can be as high as 0.4 V and V_{OH} can be as low as 2.4 V.

LVCMOS (low-voltage CMOS)

LVTTL (low-voltage TTL)

The positioning of TTL's logic levels at the low end of the 5-V range was really quite fortuitous. As shown in Figure 3-85(b) and (c), it was possible to define the LVTTL levels to match up with TTL levels exactly. Thus, an LVTTL output can drive a TTL input with no problem, as long as its output current specifications (I_{OLmax}, I_{OHmax}) are respected. Similarly, a TTL output can drive an LVTTL input, except for the problem of driving it beyond LVTTL's 3.3-V V_{CC}, as discussed next.

Figure 3-85 Comparison of logic levels: (a) 5-V CMOS; (b) 5-V TTL, including 5-V TTL-compatible CMOS; (c) 3.3-V LVTTL; (d) 2.5-V CMOS; (e) 1.8-V CMOS.



Copyright © 1999 by John F. Wakerly Copying Prohibited

*3.13.2 5-V Tolerant Inputs

The inputs of a gate won't necessarily tolerate voltages greater than V_{CC}. This can easily occur when 5-V and 3.3-V logic families in a system. For example, 5-V CMOS devices easily produce 4.9-V outputs when lightly loaded, and both CMOS and TTL devices routinely produce 4.0-V outputs even when moderately loaded.

The maximum voltage V_{Imax} that can be tolerated by an input is listed in the "absolute maximum ratings" section of the manufacturer's data sheet. For HC devices, V_{Imax} equals V_{CC}. Thus, if an HC device is powered by a 3.3-V supply, its cannot be driven by any 5-V CMOS or TTL outputs. For VHC devices, on the other hand, V_{Imax} is 7 V; thus, VHC devices with a 3.3-V power supply may be used to convert 5-V outputs to 3.3-V levels for use with 3.3-V microprocessors, memories, and other devices in a pure 3.3-V subsystem.

Figure 3-86 explains why some inputs are 5-V tolerant and others are not. As shown in (a), the HC and HCT input structure actually contains two reverse-biased *clamp diodes*, which we haven't shown before, between each input signal and V_{CC} and ground. The purpose of these diodes is specifically to shunt any transient input signal value less than 0 through *D1* or greater than V_{CC} through *D2* to the corresponding power-supply rail. Such transients can occur as a result of transmission-line reflections, as described in Section 12.4. Shunting the so-called "undershoot" or "overshoot" to ground or V_{CC} reduces the magnitude and duration of reflections.

clamp diode

Of course, diode *D2* can't distinguish between transient overshoot and a persistent input voltage greater than V_{CC}. Hence, if a 5-V output is connected to one of these inputs, it will not see the very high impedance normally associated with a CMOS input. Instead, it will see a relatively low impedance path to V_{CC} through the now forward-biased diode *D2*, and excessive current will flow.

Figure 3-86(b) shows a 5-V tolerant CMOS input. This input structure simply omits *D2*; diode *D1* is still provided to clamp undershoot. The VHC and AHC families use this input structure.

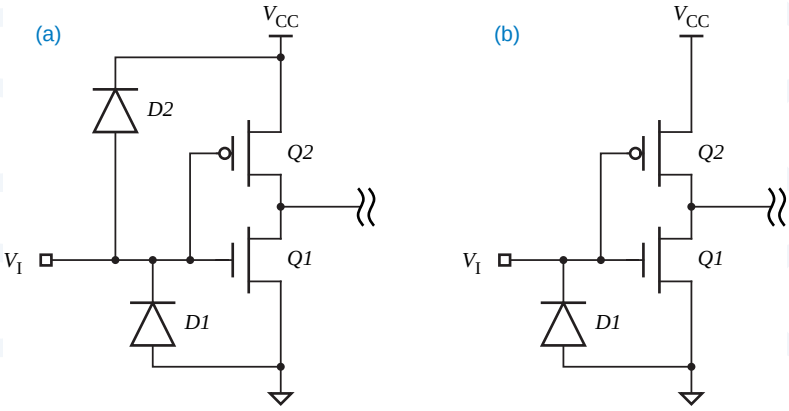


Figure 3-86
CMOS input structures: (a) non-5-V tolerant HC; (b) 5-V tolerant VHC.

Copyright © 1999 by John F. Wakerly Copying Prohibited

The kind of input structure shown in Figure 3-86(b) is necessary but not sufficient to create 5-V tolerant inputs. The transistors in a device's particular fabrication process must also be able to withstand voltage potentials higher than V_{CC}. On this basis, V_{Imax} in the VHC family is limited to 7.0 V. In many 3.3-V ASIC processes, it's not possible to get 5-V tolerant inputs, even if you're willing to give up the transmission-line benefits of diode *D2*.

*3.13.3 5-V Tolerant Outputs

Five-volt tolerance must also be considered for outputs, in particular, when both 3.3-V and 5-V three-state outputs are connected to a bus. When the 3.3-V output is in the disabled, Hi-Z state, a 5-V device may be driving the bus, and a 5-V signal may appear on the 3.3-V device's *output*.

In this situation, Figure 3-87 explains why some outputs are 5-V tolerant and others are not. As shown in (a), the standard CMOS three-state output has an *n*-channel transistor *Q1* to ground and a *p*-channel transistor *Q2* to V_{CC}. When the output is disabled, circuitry (not shown) holds the gate of *Q1* near 0 V, and the gate of *Q2* near V_{CC}, so both transistors are off and Y is Hi-Z.

Now consider what happens if V_{CC} is 3.3 V and a different device applies a 5-V signal to the output pin Y in (a). Then the drain of *Q2* (Y) is at 5 V while the gate (V_2) is still at only 3.3 V. With the gate at a lower potential than the drain, *Q2* will begin to conduct and provide a relatively low-impedance path from Y to V_{CC}, and excessive current will flow. Both HC and VHC three-state outputs have this structure and therefore are not 5-V tolerant.

Figure 3-87(b) shows a 5-V tolerant output structure. An extra *p*-channel transistor *Q3* is used to prevent *Q2* from turning on when it shouldn't. When V_{OUT} is greater than V_{CC}, *Q3* turns on. This forms a relatively low impedance path from Y to the gate of *Q2*, which now stays off because its gate voltage V_2 can no longer be below the drain voltage. This output structure is used in Texas Instruments' LVC (Low-Voltage CMOS) family.

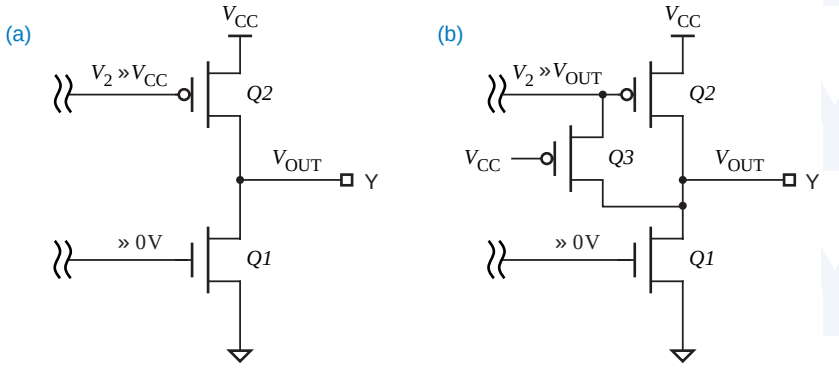


Figure 3-87
CMOS three-state output structures: (a) non-5-V tolerant HC and VHC; b) 5-V tolerant LVC.

Copyright © 1999 by John F. Wakerly Copying Prohibited

*3.13.4 TTL/LVTTL Interfacing Summary

Based on the information in the preceding subsections, TTL (5-V) and LVTTL (3.3-V) devices can be mixed in the same system subject to just three rules:

1. LVTTL outputs can drive TTL inputs directly, subject to the usual constraints on output current (I_{OLmax}, I_{OHmax}) of the driving devices.
2. TTL outputs can drive LVTTL inputs if the inputs are 5-V tolerant.
3. TTL and LVTTL three-state outputs can drive the same bus if the LVTTL outputs are 5-V tolerant.

*3.13.5 2.5-V and 1.8-V Logic

The transition from 3.3-V to 2.5-V logic will not be so easy. It is true that 3.3-V outputs can drive 2.5-V inputs as long as the inputs are 3.3-V tolerant. However, a quick look at Figure 3-85(c) and (d) on page 168 shows that V_{OH} of a 2.5-V output equals V_{IH} of a 3.3-V input. In other words, there is zero HIGH-state DC noise margin when a 2.5-V output drives a 3.3-V input, not a good situation.

level translator
level shifter

The solution to this problem is to use a *level translator or level shifter*, a device which is powered by both supply voltages and which internally boosts the lower logic levels (2.5 V) to the higher ones (3.3 V). Many of today's ASICs and microprocessors contain level translators internally, allowing them to operate with a 2.5-V or 2.7-V core and a 3.3-V pad ring, as we discussed at the beginning of this section. If and when 2.5-V discrete devices become popular, we can expect the major semiconductor vendors produce level translators as stand-alone components as well.

The next step will be a transition from 2.5-V to 1.8-V logic. Referring to Figure 3-85(d) and (e), you can see that the HIGH-state DC noise margin is actually negative when a 1.8-V output drives a 2.5-V input, so level translators will be needed in this case also.

*3.14 Emitter-Coupled Logic

The key to reducing propagation delay in a bipolar logic family is to prevent a gate's transistors from saturating. In Section 3.9.5, we learned how Schottky diodes prevent saturation in TTL gates. However, it is also possible to prevent saturation by using a radically different circuit structure, called *current-mode logic (CML)* or *emitter-coupled logic (ECL)*.

current-mode logic (CML)

Unlike the other logic families in this chapter, CML does not produce a large voltage swing between the LOW and HIGH levels. Instead, it has a small voltage swing, less than a volt, and it internally switches current between two possible paths, depending on the output state.

emitter-coupled logic (ECL)

The first CML logic family was introduced by General Electric in 1961. The concept was soon refined by Motorola and others to produce the still popular 10K and 100K *emitter-coupled logic (ECL)* families. These families are

emitter-coupled logic (ECL)

Copyright © 1999 by John F. Wakerly Copying Prohibited

extremely fast, offering propagation delays as short as 1 ns. The newest ECL family, ECLinPS (literally, ECL in picoseconds), offers maximum delays under 0.5 ns (500 ps), including the signal delay getting on and off of the IC package. Throughout the evolution of digital circuit technology, some type of ECL has always been the fastest technology for discrete, packaged logic components.

Still, commercial ECL families aren't nearly as popular as CMOS and TTL, mainly because they consume much more power. In fact, high power consumption made the design of ECL supercomputers, such as the Cray-1 and Cray-2, as much of a challenge in cooling technology as in digital design. Also, ECL has a poor speed-power product, does not provide a high level of integration, has fast edge rates requiring design for transmission-line effects in most applications, and is not directly compatible with TTL and CMOS. Nevertheless, ECL still finds its place as a logic and interface technology in very high-speed communications gear, including fiber-optic transceiver interfaces for gigabit Ethernet and Asynchronous Transfer Mode (ATM) networks.

*3.14.1 Basic CML Circuit

differential amplifier

The basic idea of current-mode logic is illustrated by the inverter/buffer circuit in Figure 3-88. This circuit has both an inverting output (OUT1) and a noninverting output (OUT2). Two transistors are connected as a *differential amplifier* with a common emitter resistor. The supply voltages for this example are $V_{CC} = 5.0$, $V_{BB} = 4.0$, and $V_{EE} = 0$ V, and the input LOW and HIGH levels are defined to be 3.6 and 4.4 V. This circuit actually produces output LOW and HIGH levels that are 0.6 V higher (4.2 and 5.0 V), but this is corrected in real ECL circuits.

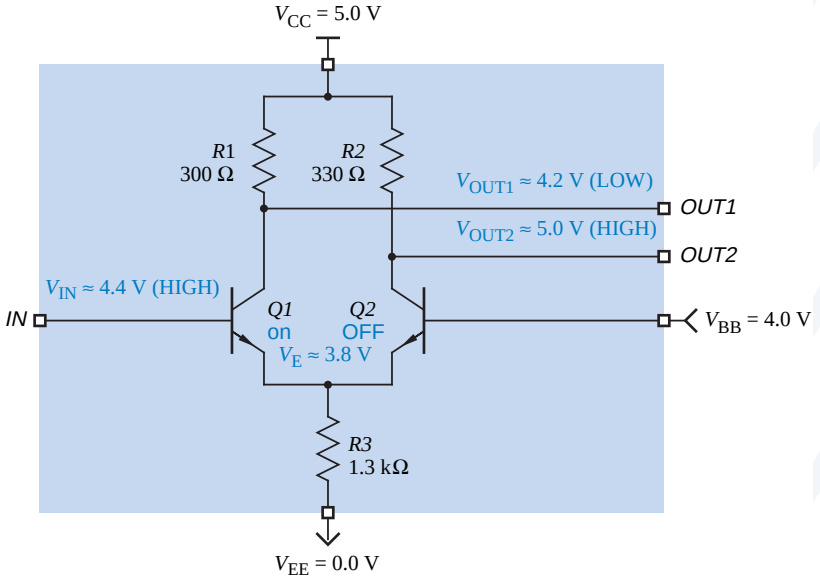


Figure 3-88
Basic CML inverter/buffer circuit with input HIGH.

Copyright © 1999 by John F. Wakerly Copying Prohibited

When V_{IN} is HIGH, as shown in the figure, transistor *Q1* is on, but not saturated, and transistor *Q2* is OFF. This is true because of a careful choice of resistor values and voltage levels. Thus, V_{OUT2} is pulled to 5.0 V (HIGH) through *R2*, and it can be shown that the voltage drop across *R1* is about 0.8 V so that V_{OUT1} is about 4.2 V (LOW).

When V_{IN} is LOW, as shown in Figure 3-89, transistor *Q2* is on, but not saturated, and transistor *Q1* is OFF. Thus, V_{OUT1} is pulled to 5.0 V through *R1*, and it can be shown that V_{OUT2} is about 4.2 V.

differential outputs

The outputs of this inverter are called *differential outputs* because they are always complementary, and it is possible to determine the output state by looking at the difference between the output voltages ($V_{OUT1} - V_{OUT2}$) rather than their absolute values. That is, the output is 1 if ($V_{OUT1} - V_{OUT2}$) > 0, and it is 0 if ($V_{OUT1} - V_{OUT2}$) > 0. It is possible to build input circuits with two wires per logical input that define the logical signal value in this way; these are called *differential inputs*

differential inputs

Differential signals are used in most ECL "interfacing" and "clock distribution" applications because of their low skew and high noise immunity. They are "low skew" because the timing of a 0-to-1 or 1-to-0 transition does not depend critically on voltage thresholds, which may change with temperature or between devices. Instead, the timing depends only on when the voltages cross over relative to each other. Similarly, the "relative" definition of 0 and 1 provides outstanding noise immunity, since noise created by variations in the power supply or coupled from external sources tend to be *common-mode signals* that affect both differential signals similarly, leaving the difference value unchanged.

common-mode signals

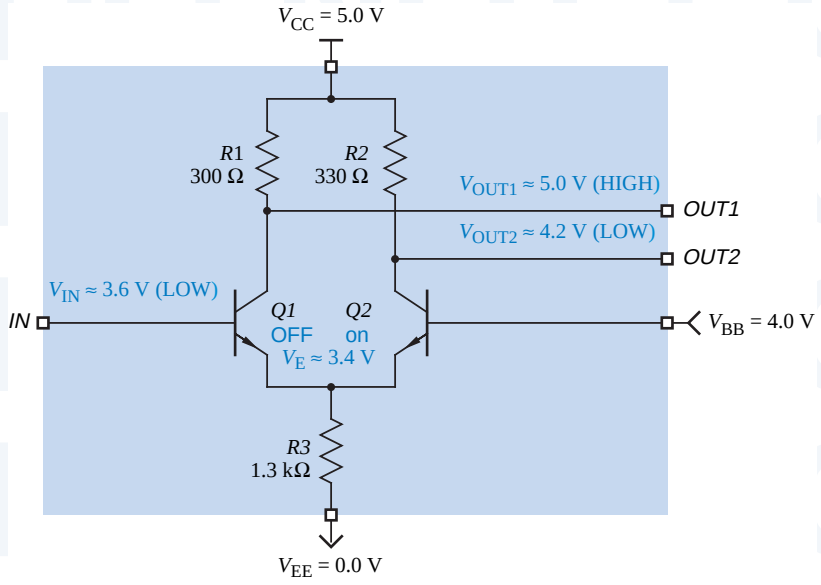


Figure 3-89
Basic CML inverter/buffer circuit with input LOW.

Copyright © 1999 by John F. Wakerly Copying Prohibited

single-ended input

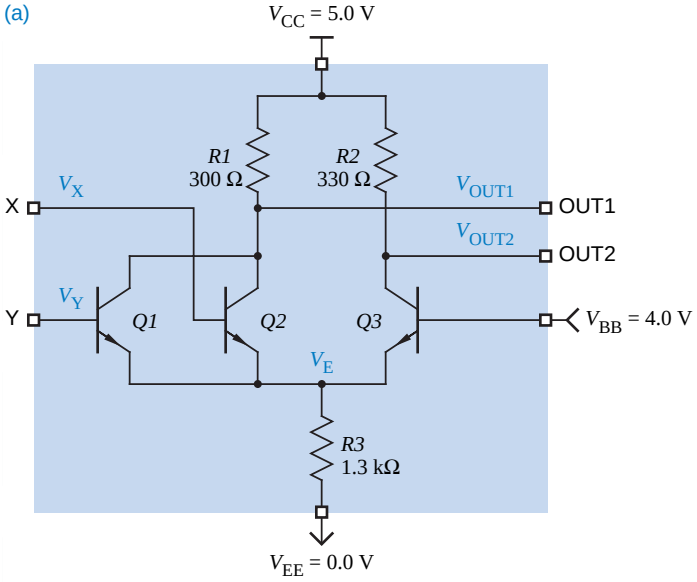
It is also possible, of course, to determine the logic value by sensing the absolute voltage level of one input signal, called a *single-ended input*. Single-ended signals are used in most ECL "logic" applications to avoid the obvious expense of doubling the number of signal lines. The basic CML inverter in Figure 3-89 has a single-ended input. It always has both "outputs" available internally; the circuit is actually either an inverter or a non-inverting buffer depending on whether we use OUT1 or OUT2.

To perform logic with the basic circuit of Figure 3-89, we simply place additional transistors in parallel with *Q1*, similar to the approach in a TTL NOR gate. For example, Figure 3-90 shows a 2-input CML OR/NOR gate. If any input is HIGH, the corresponding input transistor is active, and V_{OUT1} is LOW (NOR output). At the same time, *Q3* is OFF, and V_{OUT2} is HIGH (OR output).

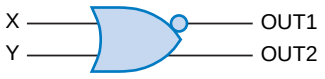
Recall that the input levels for the inverter/buffer are defined to be 3.6 and 4.4 V, while the output levels that it produces are 4.2 and 5.0 V. This is obviously

Figure 3-90 CML 2-input OR/NOR gate: (a) circuit diagram; (b) function table; (c) logic symbol; (d) truth table.

(a)



(c)



(b)

X	Y	V_X	V_Y	*Q1*	*Q2*	*Q3*	V_E	V_{OUT1}	V_{OUT2}	OUT1	OUT2
L	L	3.6	3.6	OFF	OFF	on	3.4	5.0	4.2	H	L
L	H	3.6	4.4	OFF	on	OFF	3.8	4.2	5.0	L	H
H	L	4.4	3.6	on	OFF	OFF	3.8	4.2	5.0	L	H
H	H	4.4	4.4	on	on	OFF	3.8	4.2	5.0	L	H

(d)

X	Y	OUT1	OUT2
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Copyright © 1999 by John F. Wakerly Copying Prohibited

a problem. We could put a diode in series with each output to lower it by 0.6 V to match the input levels, but that still leaves another problem—the outputs have poor fanout. A HIGH output must supply base current to the inputs that it drives, and this current creates an additional voltage drop across *R1* or *R2*, reducing the output voltage (and we don't have much margin to work with). These problems are solved in commercial ECL families, such as the 10K family described next.

*3.14.2 ECL 10K/10H Families

The packaged components in today's most popular ECL family have 5-digit part numbers of the form "10xxx" (e.g., 10102, 10181, 10209), so the family is generically called *ECL 10K*. This family has several improvements over the basic CML circuit described previously: *ECL 10K family*

- An emitter-follower output stage shifts the output levels to match the input levels and provides very high current-driving capability, up to 50 mA per output. It is also responsible for the family's name, "emitter-coupled" logic.
- An internal bias network provides V_{BB} without the need for a separate, external power supply.
- The family is designed to operate with $V_{CC} = 0$ (ground) and $V_{EE} = -5.2$ V. In most applications, ground signals are more noise-free than the power-supply signals. In ECL, the logic signals are referenced to the algebraically higher power-supply voltage rail, so the family's designers decided to make that 0 V (the "clean" ground) and use a negative voltage for V_{EE}. The power-supply noise that does appear on V_{EE} is a common-mod" signal that is rejected by the input structure's differential amplifier.
- Parts with a 10H prefix (the *ECL 10H family*) are fully voltage compensated, so they will work properly with power-supply voltages other than $V_{EE} = -5.2$ V, as we'll discuss in Section 3.14.4. *ECL 10H family*

Logic LOW and HIGH levels are defined in the ECL 10K family as shown in Figure 3-91. Note that even though the power supply is negative, ECL assigns the names LOW and HIGH to the *algebraically* lower and higher voltages, respectively.

DC noise margins in ECL 10K are much less than in CMOS and TTL, only 0.155 V in the LOW state and 0.125 V in the HIGH state. However, ECL gates do not need as much noise margin as these families. Unlike CMOS and TTL, an ECL gate generates very little power-supply and ground noise when it changes state; its current requirement remains constant as it merely steers current from one path to another. Also, ECL's emitter-follower outputs have very low impedance in either state, and it is difficult to couple noise from an external source into a signal line driven by such a low-impedance output.

Copyright © 1999 by John F. Wakerly Copying Prohibited

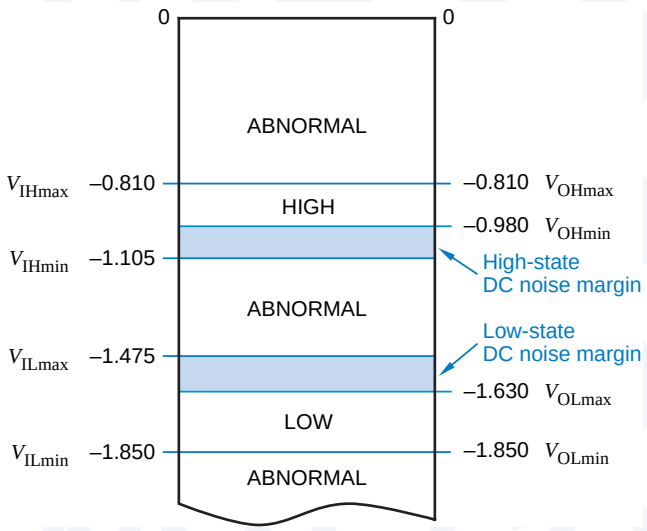


Figure 3-91
ECL 10K logic levels.

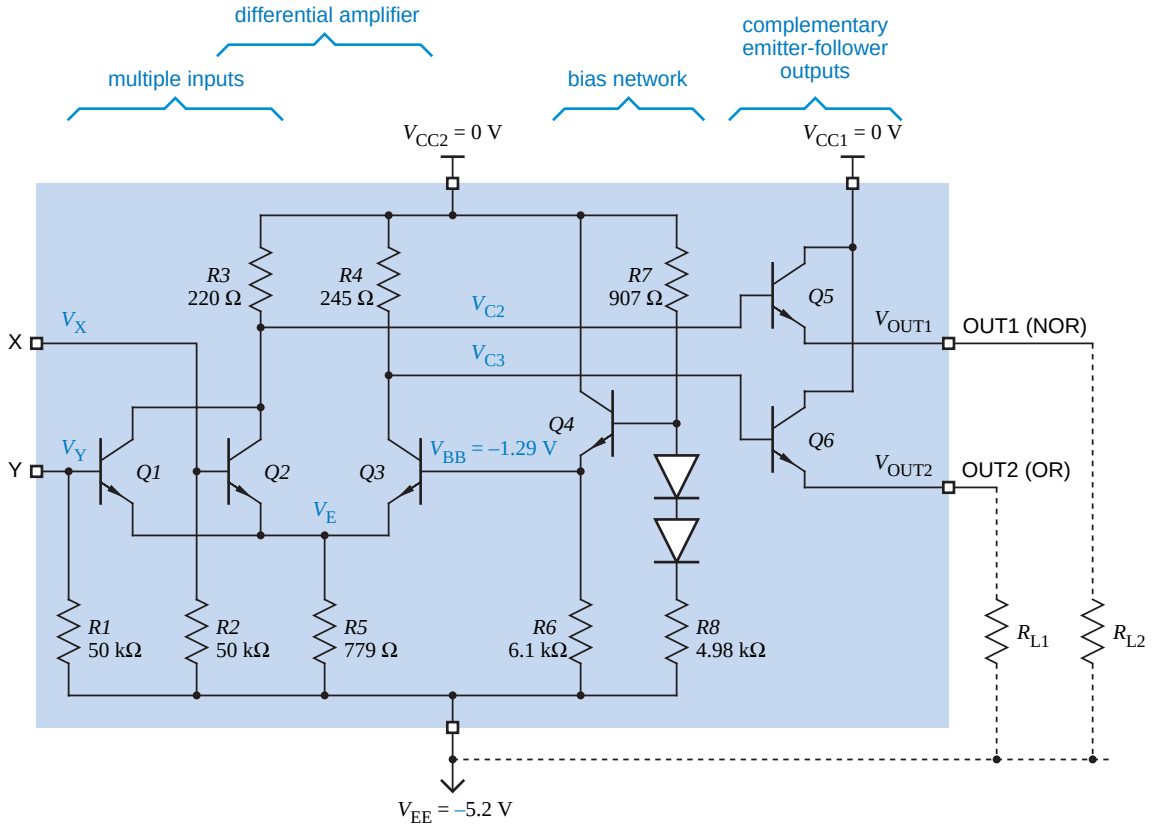
Figure 3-92(a) is the circuit for an ECL OR/NOR gate, one section of a quad OR/NOR gate with part number 10102. A pull-down resistor on each input ensures that if the input is left unconnected, it is treated as LOW. The bias network has component values selected to generate $V_{BB} = -1.29$ V for proper operation of the differential amplifier. Each output transistor, using the emitter-follower configuration, maintains its emitter voltage at one diode-drop below its base voltage, thereby achieving the required output level shift. Figure 3-92(b) summarizes the electrical operation of the gate.

The emitter-follower outputs used in ECL 10K require external pull-down resistors, as shown in the figure. The 10K family is designed to use external rather than internal pull-down resistors for good reason. The rise and fall times of ECL output transitions are so fast (typically 2 ns) that any connection longer than a few inches must be treated as a transmission line, and must be terminated as discussed in Section 12.4. Rather than waste power with an internal pull-down resistor, ECL 10K allows the designer to select an external resistor that satisfies both pull-down and transmission-line termination requirements. The simplest termination, sufficient for short connections, is to connect a resistor in the range of 270 Ω to 2 kΩ from each output to V_{EE}.

A typical ECL 10K gate has a propagation delay of 2 ns, comparable to 74AS TTL. With its outputs left unconnected, a 10K gate consumes about 26 mW of power, also comparable to a 74AS TTL gate, which consumes about 20 mW. However, the termination required by ECL 10K also consumes power, from 10 to 150 mW per output depending on the termination circuit configuration. A 74AS TTL output may or may not require a power-consuming termination circuit, depending on the physical characteristics of the application.

Copyright © 1999 by John F. Wakerly Copying Prohibited

(a)



(b)

X	Y	V_X	V_Y	Q1	Q2	Q3	V_E	V_{C2}	V_{C3}	V_{OUT1}	V_{OUT2}	OUT1	OUT2
L	L	–1.8	–1.8	OFF	OFF	on	–1.9	–0.2	–1.2	–0.9	–1.8	H	L
L	H	–1.8	–0.9	OFF	on	OFF	–1.5	–1.2	–0.2	–1.8	–0.9	L	H
H	L	–0.9	–1.8	on	OFF	OFF	–1.5	–1.2	–0.2	–1.8	–0.9	L	H
H	H	–0.9	–0.9	on	on	OFF	–1.5	–1.2	–0.2	–1.8	–0.9	L	H

(c)

X	Y	OUT1	OUT2
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

(d)

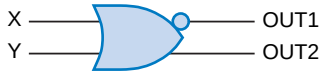


Figure 3-92 Two-input 10K ECL OR/NOR gate: (a) circuit diagram; (b) function table; (c) truth table; (d) logic symbol.

DO NOT COPY

Copyright © 1999 by John F. Wakerly Copying Prohibited

*3.14.3 ECL 100K Family

ECL 100K family

Members of the *ECL 100K family* have 6-digit part numbers of the form "100xxx" (e.g., 100101, 100117, 100170), but in general have functions different than 10K parts with similar numbers. The 100K family has the following major differences from the 10K family:

- Reduced power-supply voltage, $V_{EE} = -4.5$ V.
- Different logic levels, as a consequence of the different supply voltage.
- Shorter propagation delays, typically 0.75 ns.
- Shorter transition times, typically 0.70 ns.
- Higher power consumption, typically 40 mW per gate.

*3.14.4 Positive ECL (PECL)

We described the advantage of noise immunity provided by ECL's negative power supply ($V_{EE} = -5.2$ V or -4.5 V), but there's also a big disadvantage—today's most popular CMOS and TTL logic families, ASICs, and microprocessors all use a positive power-supply voltage, typically +5.0 V but trending to +3.3 V. Systems incorporating both ECL and CMOS/TTL devices therefore require two power supplies. In addition, interfacing between standard, negative ECL 10K or 100K logic levels and positive CMOS/TTL levels requires special level-translation components that connect to both supplies.

positive ECL (PECL)

Positive ECL (*PECL*, pronounced "peckle") uses a standard +5.0-V power supply. Note that there's nothing in the ECL 10K circuit design of Figure 3-92 that requires V_{CC} to be grounded and V_{EE} to be connected to a -5.2-V supply. The circuit will function exactly the same with V_{EE} connected to ground, and V_{CC} to a +5.2-V supply.

Thus, PECL components are nothing more than standard ECL components with V_{EE} connected to ground and V_{CC} to a +5.0-V supply. The voltage between V_{EE} and V_{CC} is a little less than with standard 10K ECL and more than with standard 100K ECL, but the 10H-series and 100K parts are voltage compensated, designed to still work well with the supply voltage being a little high or low.

Like ECL logic levels, PECL levels are referenced to V_{CC}, so the PECL HIGH level is about $V_{CC} - 0.9$ V, and LOW is about $V_{CC} - 1.7$ V, or about 4.1 V and 3.3 V with a nominal 5-V V_{CC}. Since these levels are referenced to V_{CC}, they move up and down with any variations in V_{CC}. Thus, PECL designs require particularly close attention to power distribution issues, to prevent noise on V_{CC} from corrupting the logic levels transmitted and received by PECL devices.

Recall that CML/ECL devices produce differential outputs and can have differential inputs. A differential input is relatively insensitive to the absolute voltage levels of an input-signal pair, and only to their difference. Therefore, differential signals can be used quite effectively in PECL applications to ease the noise concerns raised in the preceding paragraph.

Copyright © 1999 by John F. Wakerly Copying Prohibited

It is also quite common to provide differential PECL-compatible inputs and outputs on CMOS devices, allowing a direct interface between the CMOS device and a device such as a fiber-optic transceiver that expects ECL or PECL levels. In fact, as CMOS circuits have migrated to 3.3-V power supplies, it has even been possible to build PECL-like differential inputs and outputs that are simple referenced to the 3.3-V supply instead of a 5-V supply.

References

Students who need to study the basics may wish to consult "Electrical Circuits Review" by Bruce M. Fleischer. This 20-page tutorial covers all of the basic circuit concepts that are used in this chapter. It appears both as an appendix in this book's first edition and as a PDF file on its web page, www.ddpp.com.

If you're interested in history, a nice introduction to all of the early bipolar logic families can be found in *Logic Design with Integrated Circuits* by William E. Wickes (Wiley-Interscience, 1968). The classic introduction to TTL electrical characteristics appeared in *The TTL Applications Handbook*, edited by Peter Alfke and Ib Larsen (Fairchild Semiconductor, 1973). Early logic designers also enjoyed *The TTL Cookbook* by Don Lancaster.

For another perspective on the electronics material in this chapter, you can consult almost any modern electronics text. Many contain a much more analytical discussion of digital circuit operation; for example, see *Microelectronics* by J. Millman and A. Grabel (McGraw-Hill, 1987, 2nd ed.). Another good introduction to ICs and important logic families can be found in *VLSI System Design* by Saburo Muroga (Wiley, 1982). For NMOS and CMOS circuits in particular, two good books are *Introduction to VLSI Systems* by Carver Mead and Lynn Conway (Addison-Wesley, 1980) and *Principles of CMOS VLSI Design* by Neil H. E. Weste and Kamran Eshraghian (Addison-Wesley, 1993).

Characteristics of today's logic families can be found in the data books published by the device manufacturers. Both Texas Instruments and Motorola publish comprehensive data books for TTL and CMOS devices, as listed in Table 3-13. Both manufacturers keep up-to-date versions of their data books on the web, at www.ti.com and www.mot.com. Motorola also provides a nice introduction to ECL design in their *MECL System Design Handbook* (publ. HB205, rev. 1, 1988).

Howie Johnson?

BeeBop?

The JEDEC standards for digital logic levels can be found on JEDEC's web site, www.jedec.org. (Joint Electron Device Engineering Council). The JEDEC standards for 3.3-V, 2.5-V, and 1.8-V logic were published in 1994, 1995, and 1997, respectively.

Copyright © 1999 by John F. Wakerly Copying Prohibited

Table 3-13 Manufacturers' logic data books.

Manufacturer	Order number	Topics	Title	Year
Texas Instrument	SDLD001	74, 74S, 74LS TTL	*TTL Logic Data Book*	1988
Texas Instrument	SDAD001C	74AS, 74ALS TTL	*ALS/AS Logic Data Book*	1995
Texas Instrument	SDFD001B	74F TTL	*F Logic Data Book*	1994
Texas Instrument	SCLD001D	74HC, 74HCT CMOS	*HC/HCT Logic Data Book*	1997
Texas Instrument	SCAD001D	74AC, 74ACT CMOS	*AC/ACT Logic Data Book*	1997
Texas Instrument	SCLD003A	74AHC, 74AHCT CMOS	*AHC/AHCT Logic Data Book*	1997
Motorola	DL121/D	74F, 74LSTTL	*Fast and LSTTL Data*	1989
Motorola	DL129/D	74HC, 74HCT	*High-Speed CMOS Data*	1988
Motorola	DL138/D	74AC, 74ACT	*FACT Data*	1988
Motorola	DL122/D	10K ECL	*MECL Device Data*	1989

After seeing the results of last few decades' amazing pace of development in digital electronics, it's easy to forget that logic circuits had an important place in technologies that came before the transistor. In Chapter 5 of *Introduction to the Methodology of Switching Circuits* (Van Nostrand, 1972), George J. Klir shows how logic can be (and has been) performed by a variety of physical devices, including relays, vacuum tubes, and pneumatic systems.

Drill Problems

3.1 A particular logic family defines a LOW signal to be in the range 0.0–0.8 V, and a HIGH signal to be in the range 2.0–3.3 V. Under a positive-logic convention, indicate the logic value associated with each of the following signal levels:

(a) 0.0 V (b) 3.0 V (c) 0.8 V (d) 1.9 V
(e) 2.0 V (f) 5.0 V (g) –0.7 V (h) –3.0 V

3.2 Repeat Drill 3.1 using a negative-logic convention.

3.3 Discuss how a logic buffer amplifier is different from an audio amplifier.

3.4 Is a buffer amplifier equivalent to a 1-input AND gate or a 1-input OR gate?

3.5 True or false: For a given set of input values, a NAND gate produces the opposite output as a NOR gate.

3.6 True or false: The Simpsons are a bipolar logic family.

3.7 Write two completely different definitions of "gate" used in this chapter.

3.8 What kind of transistors are used in CMOS gates?

3.9 (Electrical engineers only.) Draw an equivalent circuit for a CMOS inverter using a single-pole, double-throw relay.

Copyright © 1999 by John F. Wakerly Copying Prohibited

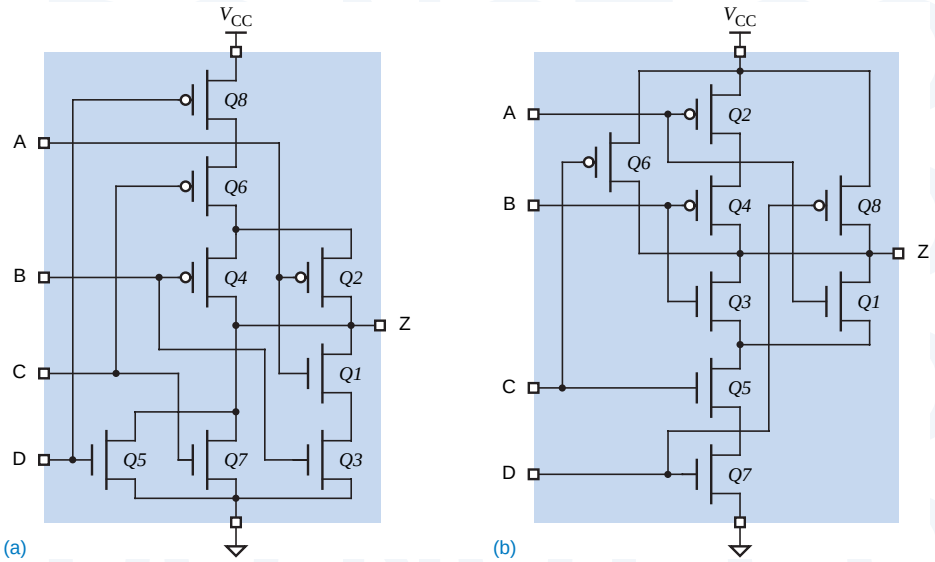


Figure X3.18

3.10 For a given silicon area, which is likely to be faster, a CMOS NAND gate or a CMOS NOR?

3.11 Define "fan-in" and "fanout." Which one are you likely to have to calculate?

3.12 Draw the circuit diagram, function table, and logic symbol for a 3-input CMOS NOR gate in the style of Figure 3-16.

3.13 Draw switch models in the style of Figure 3-14 for a 2-input CMOS NOR gate for all four input combinations.

3.14 Draw a circuit diagram, function table, and logic symbol for a CMOS OR gate in the style of Figure 3-19.

3.15 Which has fewer transistors, a CMOS inverting gate or a noninverting gate?

3.16 Name and draw the logic symbols of four different 4-input CMOS gates that each use 8 transistors.

3.17 The circuit in Figure X3.18(a) is a type of CMOS AND-OR-INVERT gate. Write a function table for this circuit in the style of Figure 3-15(b), and a corresponding logic diagram using AND and OR gates and inverters.

3.18 The circuit in Figure X3.18(b) is a type of CMOS OR-AND-INVERT gate. Write function table for this circuit in the style of Figure 3-15(b), and a corresponding logic diagram using AND and OR gates and inverters.

3.19 How is it that perfume can be bad for digital designers?

3.20 How much high-state DC noise margin is available in a CMOS inverter whose transfer characteristic under worst-case conditions looks like Figure 3-25? How much low-state DC noise margin is available? (Assume standard 1.5-V and 3.5-V thresholds for LOW and HIGH.)

3.21 Using the data sheet in Table 3-3, determine the worst-case LOW-state and HIGH-state DC noise margins of the 74HC00. State any assumptions required by your answer.

Copyright © 1999 by John F. Wakerly Copying Prohibited

3.22 Section 3.5 defines seven different electrical parameters for CMOS circuits. Using the data sheet in Table 3-3, determine the worst-case value of each of these for the 74HC00. State any assumptions required by your answer.

3.23 Based on the conventions and definitions in Section 3.4, if the current at a device output is specified as a negative number, is the output sourcing current or sinking current?

3.24 For each of the following resistive loads, determine whether the output drive specifications of the 74HC00 over the commercial operating range are exceeded. (Refer to Table 3-3, and use $V_{OHmin} = 2.4$ V and $V_{CC} = 5.0$ V.)

(a) 120 Ω to V_{CC} (b) 270 Ω to V_{CC} and 330 Ω to GND

(c) 1 KΩ to GND (d) 150 Ω to V_{CC} and 150 Ω to GND

(e) 100 Ω to V_{CC} (f) 75 Ω to V_{CC} and 150 Ω to GND

(g) 75 Ω to V_{CC} (h) 270 Ω to V_{CC} and 150 Ω to GND

3.25 Across the range of valid HIGH input levels, 2.0–5.0 V, at what input level would you expect the 74FCT257T (Table 3-3) to consume the most power?

3.26 Determine the LOW-state and HIGH-state DC fanout of the 74FCT257T when it drives 74LS00-like inputs. (Refer to Tables 3-3 and 3-12.)

3.27 Estimate the "on" resistances of the *p*-channel and *n*-channel output transistors of the 74FCT257T using information in Table 3-3.

3.28 Under what circumstances is it safe to allow an unused CMOS input to float?

3.29 Explain "latch up" and the circumstances under which it occurs.

3.30 Explain why putting all the decoupling capacitors in one corner of a printed-circuit board is not a good idea.

3.31 When is it important to hold hands with a friend?

3.32 Name the two components of CMOS logic gate's delay. Which one is most affected by load capacitance?

3.33 Determine the *RC* time constant for each of the following resistor-capacitor combinations:

(a) $R = 100$ Ω, $C = 50$ pF (b) $R = 330$ Ω, $C = 150$ pF

(c) $R = 1$ KΩ, $C = 30$ pF (d) $R = 4.7$ KΩ, $C = 100$ pF

3.34 Besides delay, what other characteristic(s) of a CMOS circuit are affected by load capacitance?

3.35 Explain the I_C formula in footnote 5 in Table 3-3 in terms of concepts presented in Sections 3.5 and 3.6.

3.36 It is possible to operate 74AC CMOS devices with a 3.3-volt power supply. How much power does this typically save, compared to 5-volt operation?

3.37 A particular Schmitt-trigger inverter has $V_{ILmax} = 0.8$ V, $V_{IHmin} = 2.0$ V, $V_{T+} = 1.6$ V, and $V_{T-} = 1.3$ V. How much hysteresis does it have?

3.38 Why are three-state outputs usually designed to "turn off" faster than they "turn on"?

Copyright © 1999 by John F. Wakerly Copying Prohibited

3.39 Discuss the pros and cons of larger versus smaller pull-up resistors for open-drain CMOS outputs or open-collector TTL outputs.

3.40 A particular LED has a voltage drop of about 2.0 V in the "on" state, and requires about 5 mA of current for normal brightness. Determine an appropriate value for the pull-up resistor when the LED is connected as shown in Figure 3-52.

3.41 How does the answer for Drill 3.39 change if the LED is connected as shown in Figure 3-53(a)?

3.42 A wired-AND function is obtained simply by tying two open-drain or open-collector outputs together, without going through another level of transistor circuitry. How is it, then, that a wired-AND function can actually be slower than a discrete AND gate? (*Hint:* Recall the title of a Teenage Mutant Ninja Turtles movie.)

3.43 Which CMOS or TTL logic family in this chapter has the strongest output driving capability?

3.44 Concisely summarize the difference between HC and HCT logic families. The same concise statement should apply to AC versus ACT.

3.45 Why don't the specifications for FCT devices include parameters like V_{OLmaxC} that apply to CMOS loads, as HCT and ACT specifications do?

3.46 How does FCT-T devices reduce power consumption compared to FCT devices?

3.47 How many diodes are required for an *n*-input diode AND gate?

3.48 True or false: A TTL NOR gate uses diode logic.

3.49 Are TTL outputs more capable of sinking current or sourcing current?

3.50 Compute the maximum fanout for each of the following cases of a TTL output driving multiple TTL inputs. Also indicate how much "excess" driving capability is available in the LOW or HIGH state for each case.

(a) 74LS driving 74LS (b) 74LS driving 74S

(c) 74S driving 74AS (d) 74F driving 74S

(e) 74AS driving 74AS (f) 74AS driving 74F

(g) 74ALS driving 74F (h) 74AS driving 74ALS

3.51 Which resistor dissipates more power, the pull-down for an unused LS-TTL NOR-gate input, or the pull-up for an unused LS-TTL NAND-gate input? Use the minimum allowable resistor value in each case.

3.52 Which would you expect to be faster, a TTL AND gate or a TTL AND-OR-INVERT gate? Why?

3.53 Describe the main benefit and the main drawback of TTL gates that use Schottky transistors.

3.54 Using the data sheet in Table 3-12, determine the worst-case LOW-state and HIGH-state DC noise margins of the 74LS00.

3.55 Section 3.10 defines eight different electrical parameters for TTL circuits. Using the data sheet in Table 3-12, determine the worst-case value of each of these for the 74LS00.

DO NOT COPY

Copyright © 1999 by John F. Wakerly Copying Prohibited

3.56 For each of the following resistive loads, determine whether the output drive specifications of the 74LS00 over the commercial operating range are exceeded. (Refer to Table 3-12, and use $V_{OLmax} = 0.5$ V and $V_{CC} = 5.0$ V.)

(a) 470 Ω to V_{CC} (b) 330 Ω to V_{CC} and 470 Ω to GND
(c) 10 KΩ to GND (d) 390 Ω to V_{CC} and 390 Ω to GND
(e) 600 Ω to V_{CC} (f) 510 Ω to V_{CC} and 510 Ω to GND
(g) 4.7 KΩ to GND (h) 220 Ω to V_{CC} and 330 Ω to GND

3.57 Compute the LOW-state and HIGH-state DC noise margins for each of the following cases of a TTL output driving a TTL-compatible CMOS input, or vice versa.

(a) 74HCT driving 74LS (b) 74VHCT driving 74AS
(c) 74LS driving 74HCT (d) 74S driving 74VHCT

3.58 Compute the maximum fanout for each of the following cases of a TTL-compatible CMOS output driving multiple inputs in a TTL logic family. Also indicate how much "excess" driving capability is available in the LOW or HIGH state for each case.

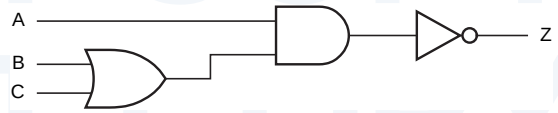
(a) 74HCT driving 74LS (b) 74HCT driving 74S
(c) 74VHCT driving 74AS (d) 74VHCT driving 74LS

3.59 For a given load capacitance and transition rate, which logic family in this chapter has the lowest dynamic power dissipation?

Exercises

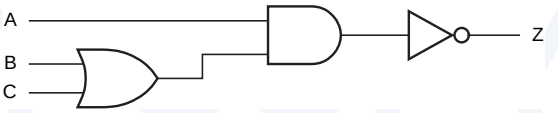
3.60 Design a CMOS circuit that has the functional behavior shown in Figure X3.60. (*Hint:* Only six transistors are required.)

Figure X3.60



3.61 Design a CMOS circuit that has the functional behavior shown in Figure X3.61. (*Hint:* Only six transistors are required.)

Figure X3.61



3.62 Draw a circuit diagram, function table, and logic symbol in the style of Figure 3-19 for a CMOS gate with two inputs A and B and an output Z, where Z = 1 if A = 0 and B = 1, and Z = 0 otherwise. (*Hint:* Only six transistors are required.)

3.63 Draw a circuit diagram, function table, and logic symbol in the style of Figure 3-19 for a CMOS gate with two inputs A and B and an output Z, where

Copyright © 1999 by John F. Wakerly Copying Prohibited

Z = 0 if A = 1 and B = 0, and Z = 1 otherwise. (*Hint:* Only six transistors are needed.)

3.64 Draw a figure showing the logical structure of an 8-input CMOS NOR gate, assuming that at most 4-input gate circuits are practical. Using your general knowledge of CMOS electrical characteristics, select a circuit structure that minimizes the NOR gate's propagation delay for a given area of silicon, and explain why this is so.

3.65 The circuit designers of TTL-compatible CMOS families presumably could have made the voltage drop across the "on" transistor under load in the HIGH state as little as it is in the LOW state, simply by making the *p*-channel transistors bigger. Why do you suppose they didn't bother to do this?

3.66 How much current and power are "wasted" in Figure 3-32(b)?

3.67 Perform a detailed calculation of V_{OUT} in Figures 3-34 and 3-33. (*Hint:* Create a Thévenin equivalent for the CMOS inverter in each figure.)

3.68 Consider the dynamic behavior of a CMOS output driving a given capacitive load. If the resistance of the charging path is double the resistance of the discharging path, is the rise time exactly twice the fall time? If not, what other factors affect the transition times?

3.69 Analyze the fall time of the CMOS inverter output of Figure 3-37, assuming that $R_L = 1\ k\Omega$ and $V_L = 2.5$ V. Compare your answer with the results of Section 3.6.1 and explain.

3.70 Repeat Exercise 3.68 for rise time.

3.71 Assuming that the transistors in an FCT CMOS three-state buffer are perfect, zero-delay on-off devices that switch at an input threshold of 1.5 V, determine the value of t_{PLZ} for the test circuit and waveforms in Figure 3-24. (*Hint:* You have to determine the time using an *RC* time constant.) Explain the difference between your result and the specifications in Table 3-3.

3.72 Repeat Exercise 3.70 for t_{PHZ}.

3.73 Using the specifications in Table 3-6, estimate the "on" resistances of the *p*-channel and *n*-channel transistors in 74AC-series CMOS logic.

3.74 Create a 4×4×2×2 matrix of worst-case DC noise margins for the following CMOS interfacing situations: an (HC, HCT, VHC, or VHCT) output driving an (HC, HCT, VHC, or VHCT) input with a (CMOS, TTL) load in the (LOW, HIGH) state; Figure X3.74 illustrates. (*Hints:* There are 64 different combinations to examine, but many give identical results. Some combinations yield negative margins.)

3.75 In the LED example in Section 3.7.5, a designer chose a resistor value of 300 Ω, and found that the open-drain gate was able to maintain its output at 0.1 V while driving the LED. How much current flows through the LED, and how much power is dissipated by the pull-up resistor in this case?

3.76 Consider a CMOS 8-bit binary counter (Section 8.4) clocked at 16 MHz. For the purposes of computing dynamic power dissipation, what is the transition frequency of least significant bit? Of the most significant bit? For the purposes of

Copyright © 1999 by John F. Wakerly Copying Prohibited

Figure X3.74

Output \ Input	HC		HCT		VHC		VHCT	
HC	CL	TL	CL	TL	CL	TL	CL	TL
	CH	TH	CH	TH	CH	TH	CH	TH
HCT	CL	TL	CL	TL	CL	TL	CL	TL
	CH	TH	CH	TH	CH	TH	CH	TH
VHC	CL	TL	CL	TL	CL	TL	CL	TL
	CH	TH	CH	TH	CH	TH	CH	TH
VHCT	CL	TL	CL	TL	CL	TL	CL	TL
	CH	TH	CH	TH	CH	TH	CH	TH

Key:
CL = CMOS load, LOW
CH = CMOS load, HIGH
TL = TTL load, LOW
TH = TTL load, HIGH

determining the dynamic power dissipation of the eight output bits, what frequency should be used?

3.77 Using only AND and NOR gates, draw a logic diagram for the logic function performed by the circuit in Figure 3-55.

3.78 Calculate the approximate output voltage at Z in Figure 3-56, assuming that the gates are HCT-series CMOS.

3.79 Redraw the circuit diagram of a CMOS 3-state buffer in Figure 3-48 using actual transistors instead of NAND, NOR, and inverter symbols. Can you find a circuit for the same function that requires a smaller total number of transistors? If so, draw it.

3.80 Modify the CMOS 3-state buffer circuit in Figure 3-48 so that the output is in the High-Z state when the enable input is HIGH. The modified circuit should require no more transistors than the original.

3.81 Using information in Table 3-3, estimate how much current can flow through each output pin when the outputs of two different 74FCT257Ts are fighting.

3.82 A computer system made by the Green PC Company had ten LED "status OK" indicators, each of which was turned on by an open-collector output in the style of Figure 3-52. However, in order to save a few cents, the logic designer connected the anodes of all ten LEDs together and replaced the ten, now parallel, 300-Ω pull-up resistors with a single 30-Ω resistor. This worked fine in the lab, but a big problem was found after volume shipments began. Explain.

3.83 Show that at a given power-supply voltage, an FCT-type I_{CCD} specification can be derived from an HCT/ACT-type C_{PD} specification, and vice versa.

3.84 If both *VZ* and *V_B* in Figure 3-65(b) are 4.6 V, can we get $V_C = 5.2$ V? Explain.

3.85 Modify the program in Table 3-10 to account for leakage current in the OFF state.

3.86 Assuming "ideal" conditions, what is the minimum voltage that will be recognized as a HIGH in the TTL NAND gate in Figure 3-75 with one input LOW and the other HIGH?

3.87 Assuming "ideal" conditions, what is the maximum voltage that will be recognized as a LOW in the TTL NAND gate in Figure 3-75 with both inputs HIGH?

3.88 Find a commercial TTL part that can source 40 mA in the HIGH state. What is its application?

Copyright © 1999 by John F. Wakerly Copying Prohibited

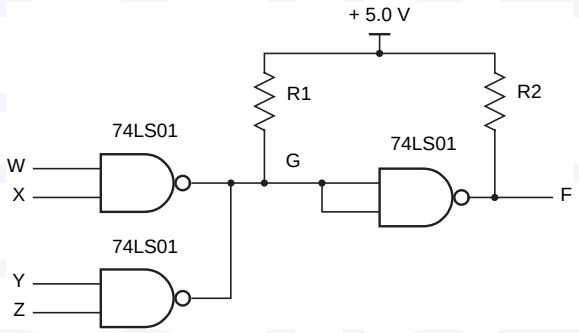


Figure X3.92

3.89 What happens if you try to drive an LED with its cathode grounded and its anode connected to a TTL totem-pole output, analogous to Figure 3-53 for CMOS?

3.90 What happens if you try to drive a 12-volt relay with a TTL totem-pole output?

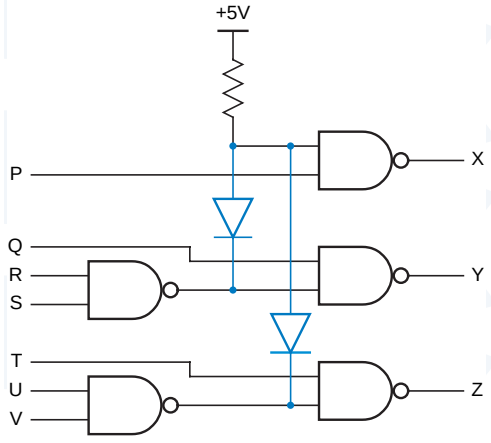
3.91 Suppose that a single pull-up resistor to +5 V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much HIGH-state DC noise margin are you providing in this case?

3.92 The circuit in Figure X3.92 uses open-collector NAND gates to perform "wired logic." Write a truth table for output signal F and, if you've read Section 4.2, a logic expression for F as a function of the circuit inputs.

3.93 What is the maximum allowable value for *R1* in Figure X3.92? Assume that a 0.7 V HIGH-state noise margin is required. The 74LS01 has the specs shown in the 74LS column of Table 3-11, except that I_{OHmax} is 100 μA, a leakage current that flows *into* the output in the HIGH state.

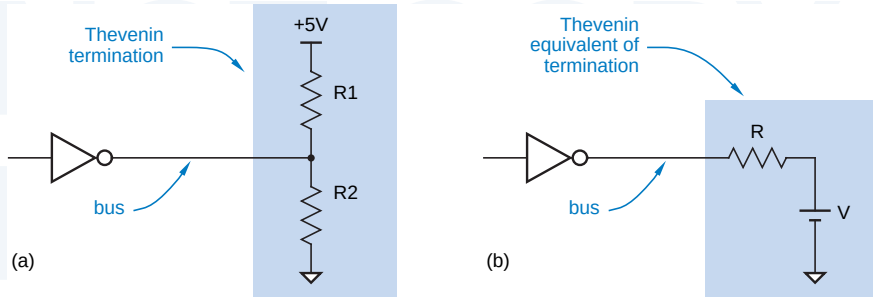
3.94 A logic designer found a problem in a certain circuit's function after the circuit had been released to production and 1000 copies of it built. A portion of the circuit is shown in Figure X3.94 in black; all of the gates are 74LS00 NAND gates. The logic designer fixed the problem by adding the two diodes shown in color. What do the diodes do? Describe both the logical effects of this change on the circuit's function and the electrical effects on the circuit's noise margins.

Figure X3.94



Copyright © 1999 by John F. Wakerly Copying Prohibited

Figure X3.95



3.95 A *Thévenin termination* for an open-collector or three-state bus has the structure shown in Figure X3.95(a). The idea is that, by selecting appropriate values of *R1* and *R2*, a designer can obtain a circuit equivalent to the termination in (b) for any desired values of *V* and *R*. The value of *V* determines the voltage on the bus when no device is driving it, and the value of *R* is selected to match the characteristic impedance of the bus for transmission-line purposes (Section 12.4). For each of the following pairs of *V* and *R*, determine the required values of *R1* and *R2*.

(a) $V = 2.75$, $R = 148.5$ (b) $V = 2.7$, $R = 180$

(c) $V = 3.0$, $R = 130$ (d) $V = 2.5$, $R = 75$

3.96 For each of the *R1* and *R2* pairs in Exercise 3.95, determine whether the termination can be properly driven by a three-state output in each of the following logic families: 74LS, 74S, 74ACT. For proper operation, the family's I_{OL} and I_{OH} specs must not be exceeded when $V_{OL} = V_{OLmax}$ and $V_{OH} = V_{OHmin}$, respectively.

3.97 Suppose that the output signal F in Figure 3.92 drives the inputs of two 74S04 inverters. Compute the minimum and maximum allowable values of *R2*, assuming that a 0.7 V HIGH-state noise margin is required.

3.98 A 74LS125 is a buffer with a three-state output. When enabled, the output can sink 24 mA in the LOW state and source 2.6 mA in the HIGH state. When disabled, the output has a leakage current of ±20 μA (the sign depends on the output voltage—plus if the output is pulled HIGH by other devices, minus if it's LOW). Suppose a system is designed with multiple modules connected to a bus, where each module has a single 74LS125 to drive the bus, and one 74LS04 to receive information on the bus. What is the maximum number of modules that can be connected to the bus without exceeding the 74LS125's specs?

3.99 Repeat Exercise 3.97, this time assuming that a single pull-up resistor is connected from the bus to +5 V to guarantee that the bus is HIGH when no device is driving it. Calculate the maximum possible value of the pull-up resistor, and the number of modules that can be connected to the bus.

3.100 Find the circuit design in a TTL data book for an actual three-state gate, and explain how it works.

3.101 Using the graphs in a TTL data book, develop some rules of thumb for derating the maximum propagation delay specification of LS-TTL under nonoptimal conditions of power-supply voltage, temperature, and loading.

Copyright © 1999 by John F. Wakerly Copying Prohibited

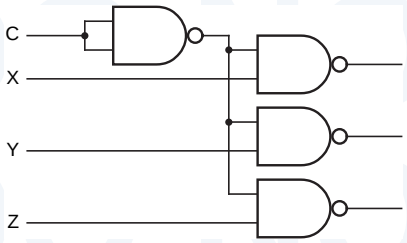


Figure X3.102

3.102 Determine the total power dissipation of the circuit in Figure 3.102 as function of transition frequency *f* for two realizations: (a) using 74LS gates; (b) using 74HC gates. Assume that input capacitance is 3 pF for a TTL gate and 7 pF for a CMOS gate, that a 74LS gate has an internal power dissipation capacitance of 20 pF, and that there is an additional 20 pF of stray wiring capacitance in the circuit. Also assume that the X, Y, and Z inputs are always HIGH, and that input C is driven with a CMOS-level square wave with frequency *f*. Other information that you need for this problem can be found in Tables 3-5 and 3-11. State any other assumptions that you make. At what frequency does the TTL circuit dissipate less power than the CMOS circuit?

3.103 It is possible to drive one or more 74AC or 74HC inputs reliably with a 74LS TTL output by providing an external resistor to pull the TTL output all the way up to V_{CC} in the HIGH state. What are the design issues in choosing a value for this pull-up resistor?

DO NOT COPY

Copyright © 1999 by John F. Wakerly Copying Prohibited

DO NOT COPY
DO NOT COPY
DO NOT COPY
DO NOT COPY
DO NOT COPY
DO NOT COPY
DO NOT COPY
DO NOT COPY
DO NOT COPY
DO NOT COPY

Copyright © 1999 by John F. Wakerly Copying Prohibited