Department of Electronics & instrumentation
Digital Logic Circuits (EC 1312)
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1) Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction (a) X -Y and (b) Y - X using 2's complements.

a)   X = 1010100
2's complement of   Y = + 0111101

                        Sum = 10010001

Discard end carry
Answer: X - Y = 0010001

b)   Y =   1000011
2's complement of   X = + 0101100

                        Sum = 1101111

There is no end carry,
Therefore the answer is Y-X = -(2's complement of 1101111) = -0010001

2). Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction (a) X -Y and (b) Y - X using 1's complements.

a). X - Y = 1010100 - 1000011

                              X =   1010100
1's complement of   Y = + 0111100

       Sum = 10010000
End -around carry   = +   1

Answer: X - Y = 0010001

b). Y - X = 1000011 - 1010100

                              Y =   1000011
1's complement of   X = + 0101011

       Sum = + 1101110

There is no end carry.
Therefore the answer is Y - X = -(1's complement of 1101110) = -0010001

3). What is meant by parity bit?
        A parity bit is an extra bit included with a message to make the total number of 1's either even or odd. Consider the following two characters and their even and odd parity:

	With even parity	With odd parity
ASCII A = 1000001	01000001	11000001
ASCII T = 1010100	11010100	01010100

In each case we add an extra bit in the left most position of the code to produce an even number of 1's in the character for even parity or an odd number of 1's in the character for odd parity. The parity bit is helpful in detecting errors during the transmission of information from one location to another.

4).What are registers?
register is a group of binary cells. A register with n cells can store any discrete quantity of information that contains n bits. The state of a register is an n-tuple number of 1's and 0's, with each bit designating the state of one cell in the register.

5). What is meant by register transfer?
A register transfer operation is a basic operation in digital systems. It consists of transfer of binary information from one set of registers into another set of registers. The transfer may be direct from one register to another, or may pass through data processing circuits to perform an operation.

6). Define binary logic?
Binary logic consists of binary variables and logical operations. The variables are designated by the alphabets such as A, B, C, x, y, z, etc., with each variable having only two distinct values: 1 and 0. There are three basic logic operations: AND, OR, and NOT.

7). Define logic gates?
Logic gates are electronic circuits that operate on one or more input signals to produce an output signal. Electrical signals such as voltages or currents exist throughout a digital system in either of two recognizable values. Voltage- operated circuits respond to two separate voltage levels that represent a binary variable equal to logic 1 or logic 0.

8).Define duality property.
Duality property states that every algebraic expression deducible from the postulates of Boolean algebra remains valid if the operators and identity elements are interchanged. If the dual of an algebraic expression is desired, we simply interchange OR and AND operators and replace 1's by 0's and 0's by 1's.

9).Find the complement of the functions $F_1 = x'yz' + x'y'z$ and $F_2 = x(y'z' + yz)$. By applying De Morgan's theorem as many times as necessary.

$F1' = (x'yz' + x'y'z)' = (x'yz')'(x'y'z)' = (x + y' + z)(x + y +z')$
$F2' = [x(y'z' + yz)]' = x' + (y'z' + yz)'$
$\qquad\qquad = x' + (y'z')'(yz)'$
$\qquad\qquad = x' + (y + z)(y' + z')$

10).Find the complements of the functions $F1 = x'yz' + x'y'z$ and $F2 = x(y'z' + yz)$. by taking their duals and complementing each literal.
$F_1 = x'yz' + x'y'z$
The dual of F1 is $(x' + y + z')(x' + y' + z)$
Complementing each literal: $(x + y' + z)(x + y + z')$
$F_2 = x(y'z' + yz)$.
The dual of F2 is $x + (y' + z')(y + z)$.
Complement of each literal: $x' + (y + z)(y' + z')$

11).State De Morgan's theorem.

   De Morgan suggested two theorems that form important part of Boolean algebra. They are,
1) The complement of a product is equal to the sum of the complements.
$$(AB)' = A' + B'$$
2) The complement of a sum term is equal to the product of the complements.
$$(A + B)' = A'B'$$

12).Reduce A.A'C

   $A.A'C = 0.c$ $[A.A' = 1]$
   $\quad\quad = 0$

13). Reduce A(A + B)
$A(A + B) = AA + AB$
$\quad\quad = A(1 + B)$ $[1 + B = 1]$
$\quad\quad = A$

14. Reduce A'B'C' + A'BC' + A'BC
$A'B'C' + A'BC' + A'BC = A'C'(B' + B) + A'B'C$
$\quad\quad\quad\quad\quad = A'C' + A'BC$ $[A + A' = 1]$
$\quad\quad\quad\quad\quad = A'(C' + BC)$ $= A'(C' + B)$ $[A + A'B = A + B]$

15.) Reduce AB + (AC)' + AB'C(AB + C)
$AB + (AC)' + AB'C(AB + C) = AB + (AC)' + AAB'BC + AB'CC$
$\quad\quad\quad\quad\quad = AB + (AC)' + AB'CC$ $[A.A' = 0]$
$\quad\quad\quad\quad\quad = AB + (AC)' + AB'C$ $[A.A = 1]$
$\quad\quad\quad\quad\quad = AB + A' + C' = AB'C$ $[(AB)' = A' + B']$
$\quad\quad\quad\quad\quad = A' + B + C' + AB'C$ $[A + AB' = A + B]$
$\quad\quad\quad\quad\quad = A' + B'C + B + C'$ $[A + A'B = A + B]$
$\quad\quad\quad\quad\quad = A' + B + C' + B'C$
$\quad\quad\quad\quad\quad = A' + B + C' + B'$
$\quad\quad\quad\quad\quad = A' + C' + 1$
$\quad\quad\quad\quad\quad = 1$ $[A + 1 = 1]$

16. Simplify the following expression Y = (A + B)(A + C')(B' + C')
$\quad\quad Y = (A + B)(A + C')(B' + C')$
$= (AA' + AC + A'B + BC)(B' + C')$ $[A.A' = 0]$
$= (AC + A'B + BC)(B' + C')$
$= AB'C + ACC' + A'BB' + A'BC' + BB'C + BCC'$
$= AB'C + A'BC'$

17).Simplify the following using De Morgan's theorem [((AB)'C)'' D]'

$[((AB)'C)'' D]'$ $= ((AB)'C)'' + D'$ $[(AB)' = A' + B']$
$\quad\quad\quad\quad = (AB)' C + D'$
$\quad\quad\quad\quad = (A' + B')C + D'$

18.Show that (X + Y' + XY)(X + Y')(X'Y) = 0

$(X + Y' + XY)(X + Y')(X'Y) = (X + Y' + X)(X + Y')(X' + Y)$ $[A + A'B = A + B]$
$\quad\quad\quad\quad\quad = (X + Y')(X + Y')(X'Y)$ $[A + A = 1]$
$\quad\quad\quad\quad\quad = (X + Y')(X'Y)$ $[A.A = 1]$
$\quad\quad\quad\quad\quad = X.X' + Y'.X'.Y$
$\quad\quad\quad\quad\quad = 0$ $[A.A' = 0]$

19).Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC

$$\begin{aligned}
ABC + ABC' + AB'C + A'BC &= AB(C + C') + AB'C + A'BC \\
&= AB + AB'C + A'BC \\
&= A(B + B'C) + A'BC \\
&= A(B + C) + A'BC \\
&= AB + AC + A'BC \\
&= B(A + C) + AC \\
&= AB + BC + AC \\
&= AB + AC + BC \qquad \text{...Proved}
\end{aligned}$$

20).Convert the given expression in canonical SOP form Y = AC + AB + BC

$$\begin{aligned}
Y &= AC + AB + BC \\
&= AC(B + B') + AB(C + C') + (A + A')BC \\
&= ABC + AB'C + ABC + ABC' + ABC + A'BC + ABC \\
&= ABC + ABC' + AB'C + A'BC \qquad [A + A = 1]
\end{aligned}$$

21).Convert the given expression in canonical POS form Y = (A + B)(B + C)(A + C)

$$\begin{aligned}
Y &= (A + B)(B + C)(A + C) \\
&= (A + B + C.C')(B + C + A.A')(A + B.B' + C) \\
&= (A + B + C)(A + B + C')(A + B + C)(A' + B + C)(A + B + C)(A + B' + C) \qquad [A + BC
\end{aligned}$$

= (A + B)(A + C)

Distributive law]

$$= (A + B + C)(A + B + C')(A' + B + C)(A' + B + C)(A + B' + C)$$

22). Find the minterms of the logical expression Y = A'B'C' + A'B'C + A'BC + ABC'

$$\begin{aligned}
Y &= A'B'C' + A'B'C + A'BC + ABC' \\
&= m0 + m1 + m3 + m6 \\
&= \sum m(0, 1, 3, 6)
\end{aligned}$$

23).Write the maxterms corresponding to the logical expression Y = (A + B + C')(A + B' + C')(A' + B' + C)

$$\begin{aligned}
Y &= (A + B + C')(A + B' + C')(A' + B' + C) \\
&= M1.M3.M6 \\
&= \prod M(1,3,6)
\end{aligned}$$

24).Convert (4021.2)₅ to its equivalent decimal.

$$\begin{aligned}
(4021.2)_5 &= 4 \times 5^3 + 0 \times 5^2 + 2 \times 5^1 + 1 \times 5^0 + 2 \times 5^{-1} \\
&= (511.4)_{10}
\end{aligned}$$

25) Using 10's complement subtract 72532 - 3250

$$\begin{aligned}
M &= \quad 72532 \\
\text{10's complement of N} &= +\ 96750
\end{aligned}$$

Sum = 169282
Discard end carry
Answer = 69282

26) What are called don't care conditions?

In some logic circuits certain input conditions never occur, therefore the corresponding output never appears. In such cases the output level is not defined, it can be either high or low. These output levels are indicated by 'X' or'd' in the truth tables and are called don't care conditions or incompletely specified functions.

27) Write down the steps in implementing a Boolean function with levels of NAND Gates?

Simplify the function and express it in sum of products.
Draw a NAND gate for each product term of the expression that has at least two literals. The inputs to each NAND gate are the literals of the term. This constitutes a group of first level gates. Draw a single gate using the AND-invert or the invert-OR graphic symbol in the second level, with inputs coming from outputs of first level gates.
A term with a single literal requires an inverter in the first level. How ever if the single literal is complemented, it can be connected directly to an input of the second level NAND gate.

28) Give the general procedure for converting a Boolean expression in to multilevel NAND diagram?

Draw the AND-OR diagram of the Boolean expression.
Convert all AND gates to NAND gates with AND-invert graphic symbols.
Convert all OR gates to NAND gates with invert-OR graphic symbols.
Check all the bubbles in the same diagram. For every bubble that is not compensated by another circle along the same line, insert an inverter or complement the input literal.

29) What are combinational circuits?

A combinational circuit consists of logic gates whose outputs at any time are determined from the present combination of inputs. A combinational circuit performs an operation that can be specified logically by a set of Boolean functions. It consists of input variables, logic gates, and output variables.

30) Give the design procedures for the designing of a combinational circuit.

The procedure involves the following steps,
From the specification of the circuit, determine the required number of inputs and outputs and assign a symbol to each.
Derive the truth table that defines the required relationships between inputs and outputs.
Obtain the simplified Boolean functions for each output as a function of the input variables.
Draw the logic diagram and verify the correctness of the design.

31) Define half adder.

A combinational circuit that performs the addition of two bits is called a half adder. A half adder needs two binary inputs and two binary outputs. The input variables designate the augend and addend bits; the output variables produce the sum and carry

32) Define full adder?

A combinational circuit that performs the adtion of three bits is a full adder.It consists of three inputs and two outputs.

33) Define binary adder.

A binary adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders constructed in cascade, with the output carry from each full adder connected to the input carry of the next full adder in the chain.

34) What is overflow?

Over flow is a problem in digital computers because the number of bits that hold the number is finite and a result that contains $n + 1$ bits cannot be accommodated. For this reason many computers detect the occurrence of an overflow, and when it occurs a corresponding flip flop is set that can be checked by the user. An overflow condition can be detected by observing the carry into sign bit position and the carry out of the sign bit position. If these two carries are not equal, an overflow has occurred.

35) Define magnitude comparator?

A magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes. The outcome of the comparison is specified by three binary variables that indicate whether a>b, A = b, or A < B.

36) What are decoders?

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. If the n bit coded information has unused combinations, he decoder may have fewer than 2^n outputs.

37) What are encoders?

An encoder is a digital circuit that performs the inverse operation of a decoder. An encoder has 2^n and n output lines. The output lines generate the binary code corresponding to the input value.

38) Define priority encoder?

A priority encoder is an encoder circuit that includes the priority function. The operation of priority encoder is such that if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

39) Define multiplexer?

A multiplexer is combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2^n input lines and n selection lines whose bit combinations determine which input is selected.

40) Define binary decoder?

A decoder which has an n- bit binary input code and a one activated output out-of -2n output code is called binary decoder. A binary decoder is used when it is necessary to activate exactly one of 2n outputs based on an n-bit input value.

41. **Represent binary number 1101 - 101 in power of 2 and find its decimal equivalent**

$N = 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3}$

$= 13.625_{10}$

42. **Convert (634) 8 to binary**

6 3 4

110 011 100

Ans = 110 011 100

43. **Convert (9 B 2 - 1A) H to its decimal equivalent.**

$N = 9 \times 16^2 + B \times 16^1 + 2 \times 16^0 + 1 \times 16^{-1} + A(10) \times 16^{-2}$

$= 2304 + 176 + 2 + 0.0625 + 0.039$

$= 2482.1_{10}$

44. **What are the different classification of binary codes?**

    1. Weighted codes

    2. Non - weighted codes

    3. Reflective codes

    . Sequential codes

    5. Alphanumeric codes

    6. Error Detecting and correcting codes.

45. **Convert 0.640625 decimal number to its octal equivalent.**

$0.640625 \times 8 = 5.125$

$0.125 \times 8 = 1.0$

Ans. $= 0.640625_{10} = 0.51$

46. **Convert 0.1289062 decimal number to its hex equivalent**

$0.1289062 \times 16 = 2.0625$

$0.0625 \times 16 = 1.0$

Ans. $= 0.21_{16}$

47. **Convert decimal number 22.64 to hexadecimal number.**

      16 22 -6

16 1 -1

0

$0.64 \times 16 = 10.24$

$0.24 \times 16 = 3.84$

$0.84 \times 16 = 13.44$

$.44 \times 16 = 7.04$

Ans. $= (16 . A 3 D 7)_{16}.3$

48. **What are the two steps in Gray to binary conversion?**

The MSB of the binary number is the same as the MSB of the gray code number. So write it down.To obtain the next binary digit, perform an exclusive OR operation b/n the bit just written down and the next gray code bit. Write down the result.

49. **Convert gray code 101011 into its binary equivalent.**

Gray Code : 1 0 1 0 1 1

Binary Code 1 1 0 0 1 0

50. Convert 10111011 is binary into its equivalent gray code.

Binary Code: 1 0 1 1 1 0 1 0 1 1
Gray code : 1 1 1 0 0 1 1 0

1 0 1 0
0 0 1 1
1 1 0 1

52. Substract (0 1 0 1) 2 from (1 0 1 1) 2

1 0 1 0
0 1 0 1
0 1 1 0

53. Find 2'S complement of (1 0 1 0 0 0 1 1) 2

0 1 0 1 1 1 0 0 1 1's Complement
+   1
0 1 0 1 1 1 0 1 0 2's complement.

54. Substract 1 1 1 0 0 1 2 from 1 0 1 0 1 1 2 using 2's complement method

1 0 1 0 1 1
+ 0 0 0 1 1 1 2's comp. of 1 1 1 0 0 1
1 1 0 0 1 0 Ans. in 2's complement form
-   0 0 1 1 1 0 Answer in true form.

55. What are the advantages of 1's complement subtraction?

1) The 1's complement subtraction can be accomplished with an binary adder. Therefore, this method is useful in arithmetic logic circuits.
2) The is complement of a number is easily obtained by inverting each bit in the number

56. Find the excess -3 code and 9's complement of the number 403 $_{10}$

4 0 3
0 1 0 0 0 0 0 0 0 0 1 1
0 0 1 1 0 0 1 1 0 0 1 1 +
0 1 1 1 0 0 1 1 0 1 1 0 excess 3 code
9's complement 1 0 0 0 1 1 0 0 1 0 0 1

57. Write the names of basic logical operators.

1. NOT / INVERT
2. AND
3. OR

58. Simplify the following expression

y = (A + B) (A = C) (B + C)
= (A A + A C + A B + B C) (B + C)
= (A C + A B + B C) (B + C)
= A B C + A C C + A B B + A B C + B B C + B C C
= A B C = A B C

59. Show that the NAND connection is not associative

The NAND connection is not associative says that

A . B . C A . B. C

A . B + C A + B C

AB + C A + BC

60. What is a Logic gate?

Logic gates are the basic elements that make up a digital system. The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logical function.

61. Write the names of Universal gates.

1. NAND gate
2. NOR gate

62. Why are NAND and NOR gates known as universal gates?

The NAND and NOR gates are known as universal gates, since any logic function can be implemented using NAND or NOR gates.

63. Define combinational logic

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called combinational logic.

64. Explain the design procedure for combinational circuits

¢ The problem definition
¢ The determination of number of available input variables & required O/P variables.
¢ Assigning letter symbols to I/O variables
¢ Obtain simplified boolean expression for each O/P.
¢ Obtain the logic diagram.

65. Define half adder and full adder

The logic circuit which performs the addition of two bits is a half adder.
The circuit which performs the addition of three bits is a full adder.

66. Define Decoder?

A decoder is a multiple - input multiple output logic circuit which converts coded inputs into coded outputs where the input and output codes are different.

67. What is binary decoder?

A decoder which has an n-bit binary i/p code and a one activated output out of 2l. output code is called binary decoder. It is used when it is necessary to activate exactly one of 2 n out puts based on an n - bit input value.

68. Define Encoder?

An encoder has 2n input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.

69. What is priority Encoder?

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

70. Define multiplexer?

Multiplexer is a digital switch. If allows digital information from several sources to be routed onto a single output line.

71. What do you mean by comparator

A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers.

72. List basic types of programmable logic devices.

1. Read only memory
2. Programmable logic Array
3. Programmable Array Logic

73. Define ROM

A read only memory is a device that includes both the decoder and the OR gates within a single IC package.

74. Define address and word:

In a ROM, each bit combination of the input variable is called on address. Each bit combination that comes out of the output lines is called a word.

75. What are the types of ROM

1. Masked ROM.
2. Programmable Read only Memory
3. Erasable Programmable Read only memory.
4. Electrically Erasable Programmable Read only Memory.

76. What is programmable logic array? How it differs from ROM?

In some cases the number of don™t care conditions is excessive, it is more economical to use a second type of LSI component called a PLA
A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generates all the minterms as in the ROM..12

77. What is mask - programmable?

With a mask programmable PLA, the user must submit a PLA PLA program table to the manufacturer.

78. What is field programmable logic array?

The second type of PLA is called a field programmable logic array. The EPLA can be programmed by the user by means of certain recommended procedures.

79. Give the comparison between prom and PLA.

PROM PLA
1. And array is fixed and or Both AND and OR arrays are
array is programmable. Programmable.
2. Cheaper and simple to use. Costliest and complex than PROMS.

80. Define even parity

In even parity the added parity bit will make the total number of 1s an even amount.

81. Define sequential circuit?

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.

82. Give the comparison between combinational circuits and sequential circuits.

Memory unit is not required Memory unity is required
Parallel adder is a combinational circuit Serial adder is a sequential circuit

83. What do you mean by present state?

The information stored in the memory elements at any given time define™s the present state of the sequential circuit.

84. What do you mean by next state?

The present state and the external inputs determine the outputs and the next state of the sequential circuit.

85. What are the types of sequential circuits?

1. Synchronous sequential circuits
2. Asynchronous sequential circuits

86. Define synchronous sequential circuit

In synchronous sequential circuits, signals can affect the memory elements only at discrete instant of time.

87. Define Asynchronous sequential circuit?

In asynchronous sequential circuits change in input signals can affect memory element at any instant of time

88. Define flip-flop

Flip - flop is a sequential device that normally. samples its inputs and changes its outputs only at times determined by clocking signal.

89. List various types of flip-flop

1] S.R. latch
2] D latch
3] Clocked J.K. flip-flop
4] T flip-flop

90. What is race around condition?

In the JK latch, the output is feedback to the input, and therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if J and K are both high then output toggles continuously. This condition is known as race around condition.

91. Define rise time and fall time?

The time required to change the voltage level from 10% to 90% is known as rise time, and the time required to change the voltage level from 90% to 10% is known as fall time.

92. Define propagation Delay?

A propagation delay is the time required to change the output after application of the input.

93. Define shift Registers

The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors.

This gives rise to a group of registers called shift registers.

94. What are the types of shift register?

1. Serial in serial out shift register?
2. Serial in parallel out shift register
3. Parallel in serial out shift register
4. Parallel in parallel out shift register
5. Bidirectional shift register shift register.

95. What are the types of counter?

1. Synchronous counter
2. Asynchronous Counter

96. What are the two models in synchronous sequential circuits.

1. Moore circuit
2. Mealy circuit

97. What is moore circuit?

When the output of the sequential circuit depends only on the present state of the flip-flop, the sequential circuit is referred to as moore circuit.

98. What is Mealy circuit?

When the output of the sequential circuit depends on both the present state of flip-flop and on the input, the sequential circuit is referred to as mealy circuit.

99. Define successor

In a state diagram, if an input sequence, x takes a machine from state si to state sj, then sj is said to be the x - successor of si.

100. Define strongly connected machine?

In a sequential machine many times certain subsets of states may not be reachable from other subsets of states, even if the machine does not contain any terminal state. However, if for every pair of states si, sj of a sequential machine, there eights an input sequence which takes M from Si to Sj then sequential machine M is said to be strongly connected.